RF synthesizer 0.1 MHz - 1 GHz

PM 5390 PM 5390 S

9452 053 90001 9452 053 90701

Service manual

9499 525 00811
8710 01/4/05

I&E
Industrial & Electro-acoustic Systems Division

PHILIPS
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Electro-acoustic Systems

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Please note

In correspondence concerning this instrument, please quote the type number and serial number as given on the type plate.

Bitte beachten

Bei Schriftwechsel über dieses Gerät wird gebeten, die Typennummer und die Gerätenummer anzugeben. Diese befinden sich auf dem Typenschild an der Rückseite des Gerätes.

Noter s. v. p.

Dans votre correspondance et dans vos réclamations se rapportant à cet appareil, veuillez toujours indiquer le numéro de type et le numéro de série qui sont marqués sur la plaquette de caractéristiques.

Important

As the instrument is an electrical apparatus, it may be operated only by trained personnel. Maintenance and repairs may also be carried out only by qualified personnel.

Wichtig

Da das Gerät ein elektrisches Betriebsmittel ist, darf die Bedienung nur durch eingewiesenes Personal erfolgen. Wartung und Reparatur dürfen nur von geschultem, fach- und sachkundigem Personal durchgeführt werden.

Important

Comme l'instrument est un équipement électrique, le service doit être assuré par du personnel qualifié. De même, l'entretien et les réparations sont à confier aux personnes suffisamment qualifiées.

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CONTENTS

1. SAFETY INSTRUCTIONS

> WARNING:
> These servicing instructions are of use by qualified personnel only. To reduce the risk of electric shock, do not perform any servicing other then that specified in the Operating Instructions unless you are fully qualified to do so.

Read these pages carefully before installation and use of the instrument.

The following clauses contain information, cautions and warnings which must be followed to ensure safe operation and to retain the instrument in a safe condition.
Adjustment, maintenance and repair of the instrument shall be carried out only by qualified personnel.

1.1. SAFETY PRECAUTIONS

For the correct and safe use of this instrument it is essential that both operating and servicing personnel follow generally-accepted safety procedures in addition to the safety precautions specified in this manual. Specific warning and caution statements, where they apply, will be found throughout the manual. Where necessary, the warning and caution statements and/or symbols are marked on the apparatus.

1.2. CAUTION AND WARNING STATEMENTS

CAUTION:
Is used to indicate correct operating or maintenance procedures in order to prevent damage to or destruction of the equipment or other property.

> WARNING:
> Calls attention to a potential danger that requires correct procedures or practices in order to prevent personal injury.

1.3. SYMBOLS

⏚ Protective earth (grounding) terminal (black)

1.4. IMPAIRED SAFETY–PROTECTION

Whenever it is likely that safety-protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation. The matter should then be referred to qualified technicians.
Safety protection is likely to be impaired if, for example, the instrument fails to perform the intended measurements or shows visible damage.

1.5. GENERAL CLAUSES

1.5.1.
> WARNING:
> The opening of covers or removal of parts, except those to which access can be gained by hand, is likely to expose live parts and accessible terminals which can be dangerous to live.

1.5.2. The instrument shall be disconnected from all voltage sources before it is opened.

1.5.3. Bear in mind that capacitors inside the instrument can hold their charge even if the instrument has been separated from all voltage sources.

1.5.4.
> WARNING:
> Any interruption of the protective earth conductor inside or outside the instrument, or disconnection of the protective earth terminal, is likely to make the instrument dangerous.
> Intentional interruption is prohibited.

1.5.5. Components which are important for the safety of the instrument may only be renewed by components obtained through your local Philips organisation (see also chapter 8).

1.5.6. After repair and maintenance in the primary circuit, safety inspection and tests, as mentioned in chapter 8, have to be performed.

2. OPERATING PRINCIPLE

2.1. BASIC PRINCIPLE OF OPERATION, fig. 30 a

The operation of the PM 5390 1 GHz RF synthesizer is based on the principle of **indirect synthesis**; frequencies are generated by VCOs **(Voltage Controlled Oscillators)** in digital **Phase-Locked Loops** (PLL).

Four of the six frequency ranges –for frequencies from 340 to 1020 MHz– are generated by the main oscillator VCO 1a ... 1d. Mixer oscillators VCO 2a and 2b generate 4 fixed frequencies for mixing with the corresponding 4 frequency ranges of the main oscillator.

The two lower frequency ranges from 0.1 to 340 MHz are generated by mixing VCO 1a or VCO 1c (assisted by VCO 2 just mentioned) with the fixed 510 MHz frequency of VCO 3. For this the output signal is switched to mixer 2.

All 3 oscillators VCO 1, VCO 2 and VCO 3 are related to the 5 MHz X-tal reference oscillator.

Frequency control operates by comparing the output signal from VCO 1, mixed with the relevant frequency generated by oscillator VCO 2, with a signal from the reference oscillator. Both signals are divided down to 1 kHz – the reference signal by a fixed reference divider and the output signal by a programmable divider controlled via ports by the microprocessor.

Also in phase-locked loop 2 the frequency is controlled via ports by setting the division factor of divider 2, in this case to 4 values for the 4 fixed frequencies.

Frequency synthesizer HEF 4750 and programmable divider 1, HEF 4751, are two ICs matched to each other. Divider 1 provides a 'fast output' FF to allow fast frequency locking and a 'slow output' FS which is used for fine phase control.

2.2. DESCRIPTION OF THE BLOCK DIAGRAM, fig. 30

The instrument works under control of the 8085 microprocessor within the central processing unit, CPU. The program memory consists of two EPROMs. On the data memory chip two further functions are implemented, i.e. a timer, generating sweep control signals, and 12 output ports for the modulation modes on the modulation interface. In the long-term data memory up to 8 complete parameter settings of the instrument can be stored and recalled. For this the BATTERY switch at the rear panel must be set to '1' (ON). The low-power CMOS RAM is backed-up by a NiCd battery pack. It ensures storage after mains switch off or in case of mains failure. Ports 2 and 3 on unit 2 and port 1 on unit 1 control all circuitries on the various units.

The keyboard/display unit 5 contains all display elements and switches (keys). Together with unit 4 it forms a sandwich pack. The central circuit on the keyboard/display interface unit 4 is the microprocessor controlled keyboard controller. This interface component produces the scan signals for the keyboard matrix and picks up the return lines, sends the data information for the 7-segment displays and controls the multiplex lines for the display positions.

The IEC bus interface is built-up in standard configuration. The data, transfer control and management signals are transferred via a flat cable from the IEEE bus connector on the small unit 6 at the rear of the instrument to the interface. The address switches are also attached to the small rear unit.

The operating principle of the oscillators VCO 1, VCO 2 and VCO 3 was already described in the previous chapter 2.1. The output of the main oscillator VCO 1 is fed to the automatic level control. Amplitude modulation can be added after this stage. Video modulation is also applied here.

Output attenuation is provided in two stages: fine adjustment is carried out by the pin-diode attenuator in the RF oscillator unit, providing a continuous range from 0 to 20 dB in 1 dB steps. Coarse attenuation is achieved outside the RF box by a 100 dB attenuator in 10 dB steps. For the PM 5390 S version a 20 dB power amplifier is added. The RF signal is then fed to the RF OUTPUT socket.

Frequency modulation signals are fed to the mixer oscillator VCO 3 in order to have a constant modulation coefficient. FM is only possible in the two lower frequency ranges up to 340 MHz, as VCO3 is active in those ranges only.

The modulation interface unit 3 processes and matches the modulation signals for the RF units, i.e. the internal and external FM, AM or VIDEO. The different modes are controlled via port 1 on unit 1. The sound part consists of a sound carrier oscillator/modulator (switched in during VIDEO), a 1 kHz oscillator and an input circuitry for external/internal sound signals for generation of AM and FM modulation.

3. CIRCUIT DESCRIPTION, FAULT FINDING, PM 5390

3.1. CENTRAL PROCESSING UNIT, IEC BUS INTERFACE; UNIT 1, fig. 37

The CPU of the PM 5390 contains the 8085 **microprocessor, the program and data memory and the output ports** for the modulation interface.

The 8085 microprocessor has a multiplexed address/data bus ADO–7 and the address bus A8–A15.

IC 317 latches the address information from ADO–7 by means of the signal ALE (adress latch enable). This address information at the output of IC 317 feeds the address inputs of the program memory, ICs 306/311 and the data memory, IC 313. The more significant address lines A8–A11, necessary for the program memory, are directly fed from the processor to the memory chips. The address lines A12–A14 from the processor are decoded by the address decoder IC 320 to 'chip enable' / 'chip select' signals for the memory circuits, ports and keyboard interface. The three input lines contain a binary information which is formed to a 1-out-of-8 signal at the output lines of this decoder.

The solder switches C and D connect pin 21 of IC 306 either to +5 V or to the address line A11 to select the PROM type 2716 or 2732 for this socket. The OR-gate 312 attaches the signals RD and 10/M to the control signal OE (output enable) for the two PROMs. This line being 'low' enables informations from the PROMs to be read by the processor.

Corresponding to modifications and technical improvements during production the software was modified several times (indicated by labels on IC 306, IC 311/unit 1).
In case of faulty PROMs normally the same software has to be replaced. Please order loaded PROMs directly via Philips Supply Center Service, Hamburg.

The integrated circuit 318 is a multifunction chip with a **RAM** of 256 bytes, two 8 bit and one 6 bit input/**output ports** and a **programmable timer.** The RAM memory is used by the processor as working storage. Ports A and B send control signals from the processor to the modulation interface, unit 3. The third port (C) senses the states of the solder switches E and G which indicate the version of the instrument (G for PM 5390 S) and of the lines OLOC and ODVD from the IEC bus controller 305. The timer within IC 318 generates sweep intervals, which result from a counter value loaded by the processor into the timer and counted down with the 30 kHz frequency of IC 302.

The timer output 318.6 sends the information 'counted down' via NOR-gate 307 to the RST 5.5 input of the processor. When this interruption is received the processor will load the timer again with a value according to the required sweep interval. The resolution of the sweep time adjustment is –with the clock frequency of 30 kHz– 1/30 000 = 33.3 μs. Timer control and data handling with the processor are performed by the control inputs CE, RD, WR, 10/M and ALE.

The integrated circuit 313 is a further **RAM memory** with a capacity of 128 bytes. This CMOS RAM stores the parameter settings; it is supplied by the built-in battery (NiCd accumulator) 805 and stores the parameters when power is switched off. The battery can be switched off by means of switch 841 at the rear of the instrument.

Attention: The storage time is dependent on the charging state of the battery:

Storage time	charging time
1 day	1 hour
5 days	3 hours
10 days	8 hours
mains supply switched off	

Attention: In order to prevent damage to the battery by complete discharge, the BATTERY switch must be set to OFF, if the instrument will not be used for approx. 3 months or more. If the battery was completely discharged by mistake it can only be loaded by desoldering from the p.c.b. and separate loading. Damaged batteries must be replaced.

During normal operation the battery is charged from the +5 V supply via diode 401 and resistor 611, with power off diode 401 blocks the current and only the ICs 303 and 313 will be supplied by the battery. Gate 303 keeps the lines $\overline{MRD}$ and $\overline{MWR}$ in a state that no information in the circuit is destroyed.

The low voltage detector 321 contains a comparator which switches the output pin 4 to 'high' when the supply voltage is decreased below +4.2; this switching level is determined by the resistors 614 and 616. During normal operation the low voltage detector enables the address decoder 320 and the processor, in the moment of power off they are disables immediately.

By means of the solder switches A and B the input line SID is fixed to 'low' in order to avoid disturbances because this input is not used.

A further part on unit 1 is the **IEC-bus interface** comprising the bi-directional bus drivers 301, 304, 308 and 314 for signal connections to the IEC bus and the IEC bus controller 305 which performs the data transfer, handshake procedure and control functions. The switches 842 - 844 at the rear of the instrument serve for setting the IEC bus address. Shift register 315 senses the states of the switches via the parallel inputs and gives this information via the serial output to the serial address input, ISR of IC 305.

When a data transfer via the IEC bus is started, IC 305 has to detect whether information received address corresponds to the address set by switches 842 - 844, the data transfer via buffers 309/310 is enabled by means of the signal ODVD attached with signal RD and the enable line from the address-decoder 320. The local/remote signal from IC 305 is sent via the buffer 309 and the NOR-gate 307 to the trap-input of the processor. Capacitor 504 and resistor 601 effect that during change from local to remote only one short pulse is fed to the trap input; the diode 402 clips negative pulses originated by this capacitor. The solder switch F serves for test purposes only: the switch being open blocks the data transfer from the IEC bus to the data bus of the processor.

The Diode 403 and capacitor 507 between the clear output OCLR, 305.33, and the input RST 6.5 of the processor lengthens the clear pulse of the controller.

The 3 MHz clock supply on unit 1 is performed with the 'clk out' signal of the processor. The clock is divided to 1.5 MHz for the IEC bus controller and the address shift register and to 30 kHz for the timer input. Clock division is done by the counter 302.

All general and detailed information about functions and fault finding in the IEC bus system can be found in the 'Philips Instrumentation System Reference Manual', 9499 997 00411.

3.2. CONTROL UNIT; UNIT 2, fig. 38

Unit 2 contains all ports, buffers and drivers to control the different circuits. The ports are fed with information from the microprocessor on unit 1 via the multiplexed address/data bus; this information is stored and sent via buffers an drivers to the reed relais and attenuators by means of which the required parameters are converted.

The ports 2 and 3 contain memory registers to store the data bus information from the processor and output buffers to drive the output lines. These lines are divided into three groups A, B and C, each of them with 8 input/output lines; in this instrument they are used only as outputs.

The output lines A0-A4 of port 305 are directly fed via connector D and buffers on the motherboard, unit 10, to the RF unit 2 for control of the programmable divider 2, ICs 308-311. The outputs A6 and A7 as well as B0-B3 send their information via inverting buffers 316 and connector D to the motherboard and control the relais 801 - 806, the contacts of which switch the supply voltages for the 6 VCOs of the main oscillator in the RF unit.

The output lines B4 and B5 control the relais 808 and 807 via the transistors 337 and 338: they switch the output signal of the pin-diode attenuator to mixer 2 and actuate VCO3 and the low-pass filter U10/U11 on the RF unit 1 for the 2 lower frequency ranges, 0.1 - 340 MHz. All these points in the RF unit require control voltages being quite accurate and without saturating voltage of transistors or drivers; therefore reed contacts are used.

The transistor 335 on unit 2 is not fitted in the standard version, but for the option PM 5390 S. The input of the transistor is driven from the port output B6; the output drives a relay which activates the 20 dB power amplifier in order to get a higher output amplitude of 1 Vrms. Actuation is done by switching the amplifier supply voltage from -12 V to +24 V.
The remaining output lines of port 2 (B7 and C0-C7) are used to control the **coarse and fine attenuator** in order to set the output amplitude from -127 dBm to -7 dBm. The lines C5-C7 are converted from TTL level at the port output to +12 V; this level is necessary to control the programmable attenuator which sets the output level in steps of 10 dBm.

Fine attenuation of the RF signal is performed by pin-diodes in the RF unit controlled by the D/A converter on unit 2. The port outputs C0-C4 feed their currents through resistors 605 - 609 into the summing point of the operational amplifier 308. The values of these resistors are weighed. 3 more lines control the pin-diode attenuator: the outputs B0' - B2', port 3, IC 309, are converted from TTL-level at the port output to 12 V level for CMOS; they control the solid state switches IC 310, by means of which the resistors 639, 652 and 653 are switched to +12 V feeding a current into the summing point of IC 308.

Thus with port 2, C0-C4, a total number of 8 lines control the D/A converter for the pin-diode attenuator, which corresponds to a resolution of 256 points; the sum of the currents will produce a voltage drop at resistor 683. Thus the output of IC 308 shows a DC-level depending on the current through resistor 683. The working point is set by resistor/potmeter 638/681, the gain by resistor 662, depending on the characteristic of the assigned pin-diode. For further details see also chapter 3.5.4.

The **programmable divider 1**, IC 301, HEF 4751, together with HEF 4750, VCO 1 and two 10/11:1 prescaler on RF unit 2 build the phase-locked loop frequency synthesizer system of the instrument, see figs. 3 and 30.

A0' - A5' of port 3, IC 309, control the programmable divider 1. Conversion from TTL- to CMOS-level is achieved by AND-gates 302 and 306, the outputs of which are connected via the pull-up resistor network 601 to +10 V. These 10 V are generated at the reference diode 401 and the resistor 604 from the 12 V supply. At the outputs FB2, SY, FB1 the +10 V are converted to ECL levels for the 10/11:1 prescalers on RF-U2: 9.5 V for high, 8.2 for low level.

The frequency of the main oscillator VCO1, mixed with VCO2 to 50 MHz - 220 MHz, is divided to provide 2 control signals for the phase comparator within IC 314; a fast 10 kHz control output FF for fast frequency locking and a slow 1 kHz control output FS for fine phase control. The division factor 50 000 - 220 000 is set by 6 ports A0' - A5', BCD coded, in a bit-parallel, digit-serial format. The second input of the phase comparator is the 10 kHz reference frequency, derived from the 5 MHz oscillator via the 500:1 divider within IC 314. The program clock is 130 kHz, derived from the 5 MHz oscillator and the 23:1 divider 4, IC 307. The division factor 23:1 is achieved by connecting the outputs of IC 307 via NAND-gate 311 to the reset input.
The function of the programmable divider and phase-locked loop is further described in chapter 3.5.3 with fig. 8.

Another function on unit 2 is the **sweep ramp generation**. The sweep time divider, binary counter 312, counts pulses sent from the timer on unit 1, input TCU. The output lines are connected to the summing point of the operational amplifier 304 via the resistors 643 - 648 the values of which are binary weighed. The currents through the resistors generate a voltage drop a resistor 635 in form of a staircase signal. The output of IC 304 is connected to the SWEEP TIME OUT socket at the rear of the instrument, where a staircase voltage from 0 to 500 mV in 50 steps of 10 mV each is available; the length of a staircase ramp, i.e. the sweep time, can be adjusted from 0.05 s to 20 s.
At each step the CPU increases the actual frequency by 1/50 of Δ frequency, starting at the set FREQUENCY and ending at FREQUENCY plus Δ FREQUENCY. Sweep is only possible within one of the subranges.
For the **sweep frequency generation** and more details about the sweep ramp generation see chapter 3.5.5.

3.3. MODULATION INTERFACE, UNIT 3, fig. 39

Processing and matching of the modulation signals for the RF units, i.e. the internal and external FM, AM or VIDEO are achieved by unit 3. The different modes are controlled via ports P1/B0-6, P1/A4-7, P1/A0-1 of CPU, unit 1, and are switched by inverters 351/352 and FET-switches 353 ... 356. These switches are supplied by -2 V at pin 7 and +12 V at pin 14.
Detailed information of the logic states and port outputs for all modulation modes is given in table fig. 1.

IC318 (U1)	PORT1 / B0 ... 6							PORT1 / A0 ... 7							
	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Pin U1	B11	B10	B9	B8	B7	B6	B5	B14	B13	B12	C26	C25	C24	C23	C22
Pin U3	5	6	7	8	9	10	11	2	3	4	1	12	not used		
ident. U3	E	F	G	H	J	K	L	B	C	D	A	H	–	–	–
AM int	1	1	1	1	1	0	0	1	0	1	1	1			
AM ext	1	1	0	1	1	0	1	1	1	1	1	1			
FM int	1	1	1	1	1	1	0	1	1	1	0	1			
FM ext	1	1	1	0	1	1	1	1	1	1	1	1			
VIDEO	1	1	1	1	0	1	1	1	1	1	1	1			
V.FM int	0	1	1	1	0	1	0	1	1	0	1	0			
V.FM ext	0	0	1	1	0	1	1	1	1	1	1	0			
V.AM int	1	1	1	1	0	1	0	0	1	0	1	0			
V.AM ext	1	0	1	1	0	1	1	0	1	1	1	0			

Fig. 1 Unit 1 and 3; logic states of port outputs for modulation modes

The **sound part** consists of a sound carrier oscillator/modulator (switched in during VIDEO), a 1 kHz oscillator and an input circuitry for external/internal sound signals for generation of AM and FM modulation.

The **1 kHz oscillator** is a RC oscillator based on the Wien-bridge principle, the components of which are 654, 535, 534, 659. A rectifier is added balancing the differential amplifier 307/1.2. So the stability of oscillation and amplitude is achieved. The oscillator is switched in by 355/L.

For external FM sound signals a decoupling preamplifier 306, 307/5, 308 is available. By means of soldering link F the required pre-emphasis of 50 μs can be obtained.
In VIDEO/FM-mode the modulation signal is applied via FET-switch 355/E to the sound carrier oscillator/modulator. In FM-mode (f = 0.1 – < 340 MHz) the FM modulation signal is applied via switches 354/H or 356/A and output FM (point 21) directly to the RF-unit 1.

In VIDEO/AM-mode the modulation signal is applied to the sound carrier oscillator/modulator via FET–switch 355/B. In mode RF carrier / AM the modulation signal is fed via IC 357 to the AM amplifier 304/4 ... 11.

The **sound carrier oscillator and -modulator** is a Colpitts-circuitry with transistor 309. The sound carrier frequency can be set to 4.5 MHz, 5.5 MHz, 6.0 MHz or 6.5 MHz by means of corresponding solder links A, B, C. For 6.5 MHz all solder links are open. Adjustment to the correct frequency is achieved by trimmer 552, 556, 560 and 564.
The frequency modulation of the sound carrier occurs by varicap 410, whereby the deviation for 5.5 MHz is adjusted by potmeter 692. The deviation of the other sound carrier frequencies depends on the capacitance ratio. Transistor 311 serves as amplitude modulator.

The VIDEO input is ac-coupled. A sync-separate circuitry (513, 614, 615, 616 and 302) separates a sync-clamp-pulse in order to clamp the external signal to ground by transistor 303. The external signal is buffered by transistor 301. By scaling resistors 619 and 620 the accurate signal level is added to the sound carrier signal to the input of signal-addition-amplifier 304/1, 2, 3, 12, 13, 14. Positive or negative video modulation is selected by solder links E or D.
Adjustment of the dc-level at the output AM/VIDEO in video mode is achieved by potmeter 631. The residual carrier signal is adjusted by 645.
Final amplification takes place in the second signal-addition-amplifier 304/4 ... 11 where the preamplified AM-signal is applied via 547. The correct working point of this stage is adjusted without any modulation by potmeter 639. During AM-mode the level of the RF carrier is reduced by 6 dB, realized by switch 353/K and resistor 633.

3.4. KEYBOARD/DISPLAY; UNIT 4, 5; figs. 40, 41

The central circuit on unit 4 is the microprocessor controlled keyboard controller P8279. This interface component produces the scan signals for the keyboard matrix and picks up the return lines, sends the data information for the 7-segment displays and controls the multiplex lines for the display positions. The LED's INT, AM, FM, VIDEO, EXT, REMOTE, SINGLE and CONT are driven from the port outputs on the CPU, unit 1, via the buffers 305 and 306 on U4.

The information from the processor is fed to the keyboard controller via the data bus AD0 – AD7; the data transfer is performed by the control signals $\overline{RD}$, $\overline{WR}$, Clk, RES and IRQ. The chip select signal $\overline{CS}$ is generated on the CPU-card from the address decoder IC 320, pin 7.

Data information for the 7-segment displays is sent via the lines OUT B0 – OUT B3 to the 7-segment decoder IC 308 which generates 7 output lines for the segments, the decimal points are driven by the outputs A1 and A2 via gate 303 or by the timer circuit IC 307 for blinking decimal points.

The scan information is contained in the four lines SL0 – SL3 which are decoded to 1-out-of-16 with the decoder 301. When the outputs of this circuit are switched on (= Low) the according display position is lit. Thus the data information at the lines a-g (7-segment) together with the according set multiplex line give the complete information for each display position. Coordination of the timing between data information and multiplex line is automatically done in the P8279.

Three of the scan lines SL0 – SL2 are used to scan the keyboard matrix. The BIN – BCD decoder 304 produces the information for the scan lines of the keyboard-matrix, the return lines are connected directly to IC 302. Pressing one of the keys effects IRQ (interrupt request) be sent to the main processor on Unit 1; after this it is possible to transfer the code of the key via the data lines AD0 – AD7 from the keyboard controller to the CPU card.

The integrated circuit 307 is a timer circuit which generates the flash-clock for the decimal points (during input) or for the digits in case of exceeding the specifications for the parameters. Flashing of the decimal points is enabled by the inputs 'FM flash' or 'VIDEO flash' being set, the blinking display positions are effected by the output $\overline{BD}$ of IC 302.

Unit 5 contains all display elements and switches (keys) and together with unit 4 forms a sandwich pack; interconnections between themselves and connections to the motherboard, unit 10, are done via CIS connectors.

3.5. RF UNITS 1 and 2; figs. 42 - 46

3.5.1. General

The frequency synthesis is a combination of system elements that results in the generation of many frequencies from one or few reference sources. The frequency accuracy and stability of the device are determined by the accuracy and stability of the crystal reference source and to a less extend the circuit.

The RF oscillator unit is the heart of this programmable frequency generator. The unit comprises the two single screened RF units 1 and 2 which are mounted together with connection board RF into the control RF box. The PM 5390 RF synthesizer is based on the principle of indirect synthesis; frequencies are generated by VCOs (Voltage Controlled Oscillators) in digital Phase-Locked Loops (PLL). A phase locked loop is basically an electronic servo loop consisting of a phase detector PD, a low-pass filter and a VCO. Its controlled oscillator phase makes it capable of locking or synchronizing with an incoming signal. If the phase changes, which indicates that the incoming frequency is changing, the phase detector output voltage increases or decreases just enough to keep the oscillator frequency the same as the incoming frequency, preserving the locked condition.

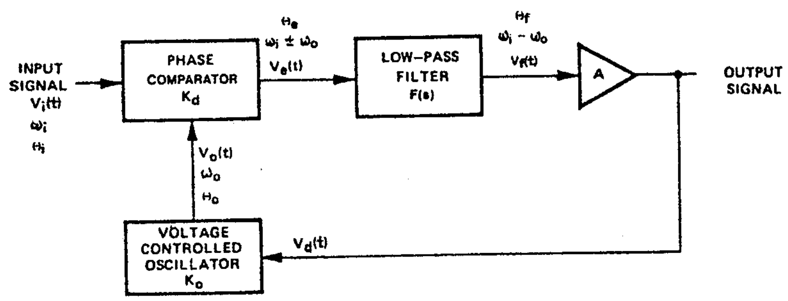


Fig. 2 Block diagram of Phase Locked Loop (PLL)

Four of the six subranges –340 to 510 MHz, 510 to 680 MHz, 680 to 850 MHz and 850 to 1020 MHz– are generated by VCO 1a ... d. To get always the same dividing range N in loop 1 the output signal f1 of VCO1 in this digital PLL is down converted by mixer 1 to 50 MHz ... 220 MHz.

Mixer oscillators VCO2 a and b generate 4 fixed frequencies for mixing with the corresponding 4 frequency ranges of the main oscillator.

The resolution of the output frequency is 1 kHz (10 kHz above 1000 MHz); so the divider N must be set between 50 000 and 200 000 in steps of 1. This is achieved by the programmable divider 1 (U2) and two 10/11:1 prescalers (RF-U2), controlled by port 3A, unit 2.

The frequency ranges from 0.1 to 170 MHz and 170 to 340 MHz are generated by mixing VCO1a or VCO1c (assisted by VCO2 just mentioned) with the fixed 510 MHz frequency of VCO3. For this the output signal is switched to mixer 2. The lowpass filter (RF-U1/U11/U12) separates unwanted mixer products.

All 3 oscillators VCO1, VCO2 and VCO3 are related to the 5 MHz X-tal reference oscillator.

Fig. 4 shows the different oscillators involved into the frequency generation from 0.1 to 1020 MHz.

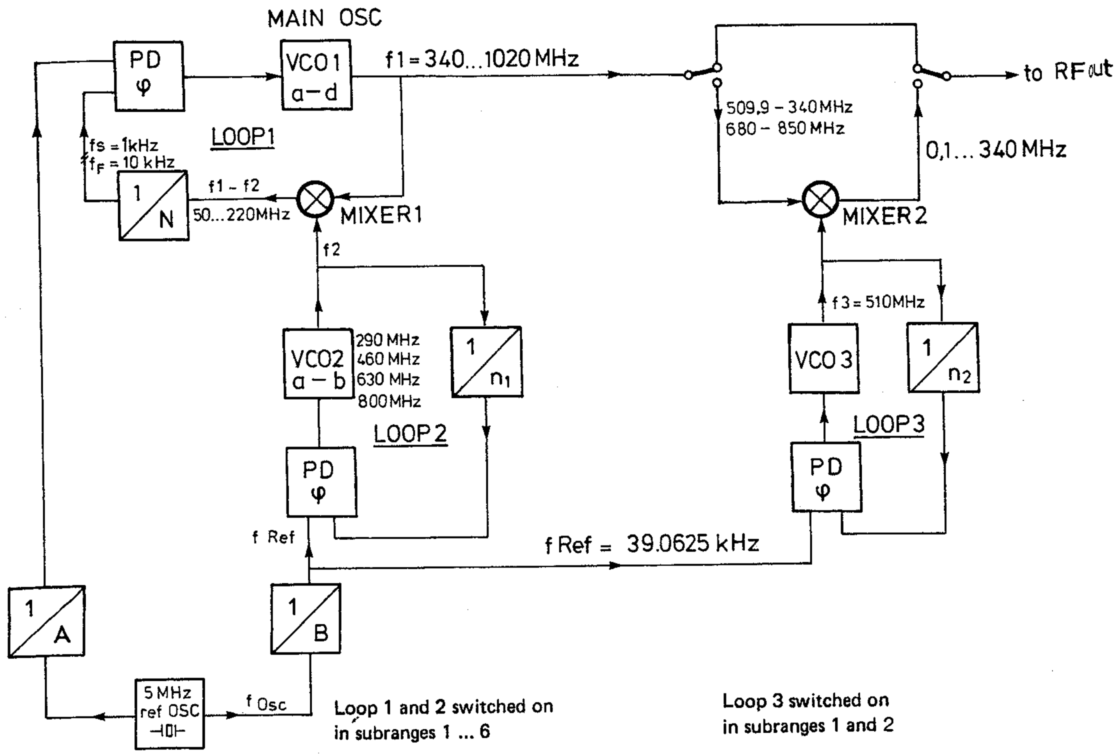


Fig. 3 Principle of RF generation PM 5390

Characteristics of indirect synthesis

Main oscillator freq. (VCO1)	f_1	= 340 ... 1020 MHz
Conversion oscillator freq. (VCO2)	f_2	= 290/460/630/800 MHz
Converted frequency	$f_1 - f_2$	= 50 ... 220 MHz
Conversion oscillator freq. (VCO3)	f_3	= 510 MHz
Reference oscillator frequency	fosc	= 5 MHz
Reference frequency slow loop 1	fs	= 1 kHz
Reference frequency fast loop 1	f_F	= 10 kHz
Reference frequency loop 2 and 3	f_{Ref}	= 39.0625 kHz

Divider settings:

Ref. divider for loop 1	A	= 5000
Divider 5	B	= 128
Progr. divider for fs	N	= 50.000 ... 220.000
Progr. divider 2	n1	= 29 x 256 at 290 MHz; 46 x 256 at 460 MHz; 63 x 256 at 630 MHz; 80 x 256 at 800 MHz
Ref. divider loop 3	n2	= 13056

The locked PLL loop 1 and 2 is represented by:

$$f1 = fosc \left\{ \frac{N}{A} + \frac{n1}{B} \right\}$$

e.g. frequency RF out (f1) = 1000 MHz

N = 200.000, A = 5000, B = 128; n1 = 80 x 256

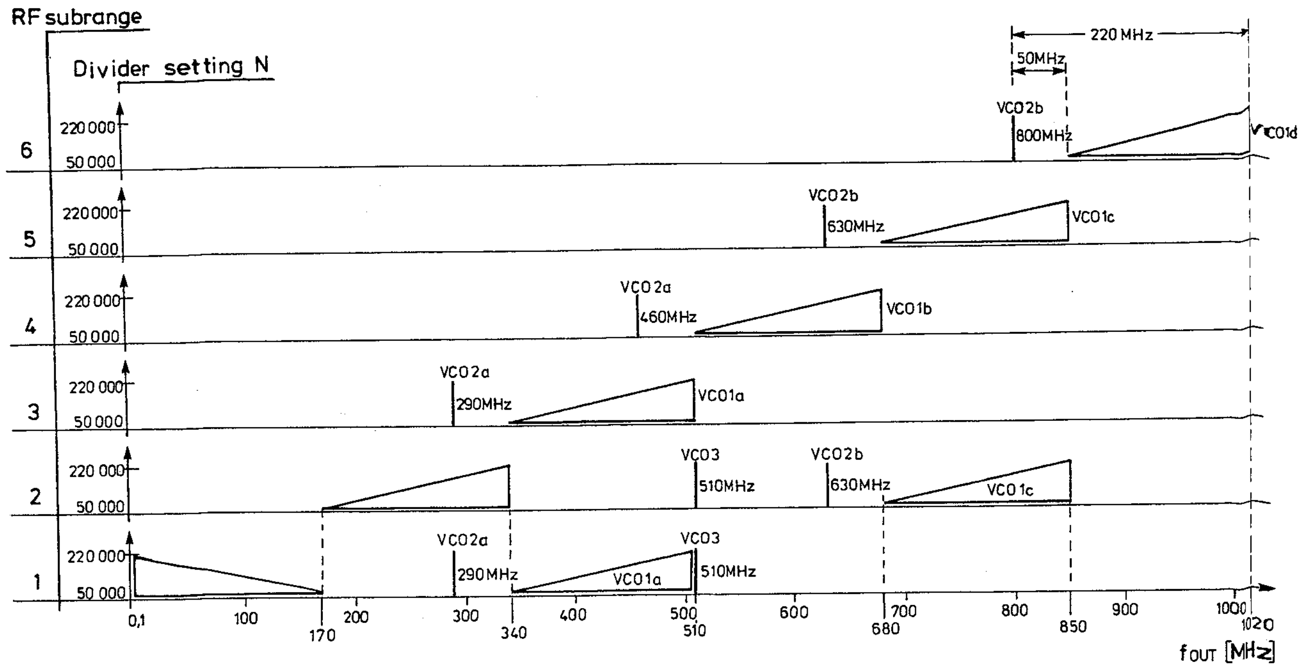


Fig. 4 RF oscillator positions, conversion oscillators

	RF unit 1								RF unit 2									
Subranges MHz	VCO1 MHz	VCO3 MHz	A ②	B ①	C ⑤	D ③	VS11 Vdc	VS21 Vdc	VCO2 MHz	f1 - f2 MHz	progr. divider 2 n1	A ⑧	B ⑩	C/D ⑨	E ⑫	F ⑪	VS12 Vdc	VS22 Vdc
0.1-170	509.9-340	510	-12V				-12	+12	290	50...220MHz	29x256		L	L	L		-12	
170-340	680-850	510			-12V		-12	-12	630	↓	63x256	L	L	L	L			-12
340-510	340-510	-	-12V				+12	-	290		29x256		L	L	L		-12	
510-680	510-680	-		-12V			+12	-	460		46x256	L		L			-12	
680-850	680-850	-			-12V		+12	-	630		63x256	L	L	L	L			-12
850-1020	850-1020	-				-12V	+12	-	800		80x256				L	L		-12

switching current: $-I_{A-D}$ ca. 7 mA ca. 7 mA

$+I_{S11}$ ca. 65 mA $-I_{S11}$ ca. 18 mA

$+I_{S21}$ ca. 10 mA $-I_{S21}$ ca. 10 mA

switching current: $-I_{S12}/-I_{S22}$ ca. 7 mA

○=pin no.

Fig. 5 RF unit 1 and 2; table of port settings

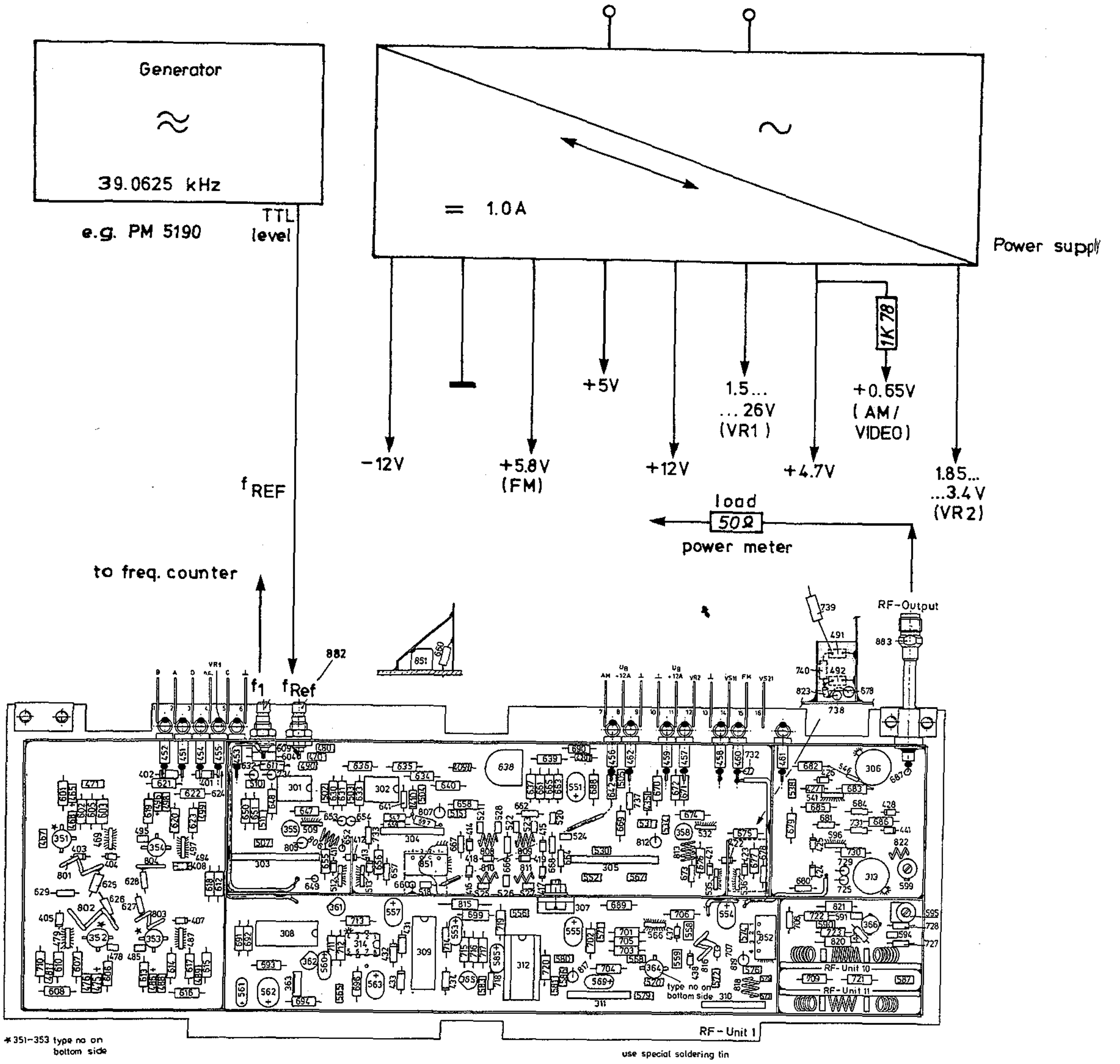


Fig. 6 Single-board test, RF unit 1 (PM 5390/5390S)

sub-range	frequency MHz	VCO 1a ... d MHz	VCO 3 MHz	A p. 2	B p. 1	C p. 5	D p. 3	VR 1 p. 4	AM/Vid p. 7	VS11 p. 14	FM p. 15	VS 21 p. 16	fREF 882	VR 2 p. 12
1	0.1 – 170	VCO1a 509.9 – 340	510	-12V				+24...+4,5V	+0.65V	-12V	+5.8V	+12V	39.0625kHz (TTL level)	+1,85...3,4V
2	170 – 340	VCO1c 680 – 850	510			-12V		ca.+5...+20V		-12V		-12V		
3	340 – 510	VCO1a 340 – 510	–	-12V				+4,5...24V		+12V		–		
4	510 – 680	VCO1b 510 – 680	–		-12V			>+1,7...24V		+12V		–	tolerance $1 \cdot 10^{-5}$	attenuation 0 ... 20 dBm
5	680 – 850	VCO1c 680 – 850	–			-12V		ca.+5...20V		+12V		–		
6	850 – 1020	VCO1d 850 – 1020	–				-12V	+3...20V		+12V		–		

Fig. 7 RF unit 1, table supply voltages

3.5.2. Phased Locked Loop terminology (PLL)

Phase Detector (PD)
A circuit which compares the input and VCO signals and produces an error voltage which is dependent on their relative phase difference. This error voltage corrects the VCO frequency during tracking. Also called Phase Comparator.

Low-Pass Filter (LPF)
A low-pass filter in the loop which permits only dc and low frequency voltages to travel around the loop. It controls the capture range and the noise and outband signal rejection characteristics.

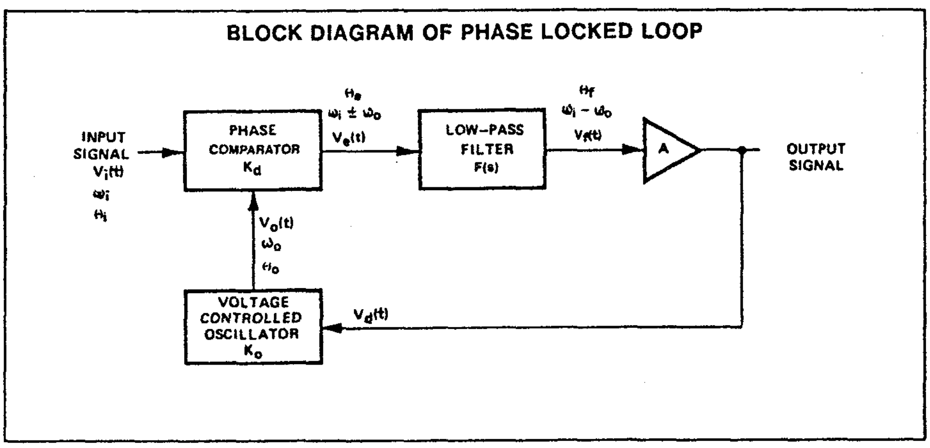
Voltage Controlled Oscillator (VCO)
An oscillator whose frequency is determined by an applied control voltage.

Lock Range ($2\omega L$)
The range of frequencies over which the loop will remain in lock. Normally the lock range is centered at the free-running frequency unless there is some non-linearity in the system which limits the frequency deviation on one side fo. The deviations from fo are referred to as the Tracking Range or Hold-in Range.

Free-Running Frequency (fo, ωo)
Also called the Center Frequency; this is the frequency at which the loop VCO operates when not locked to an input signal.

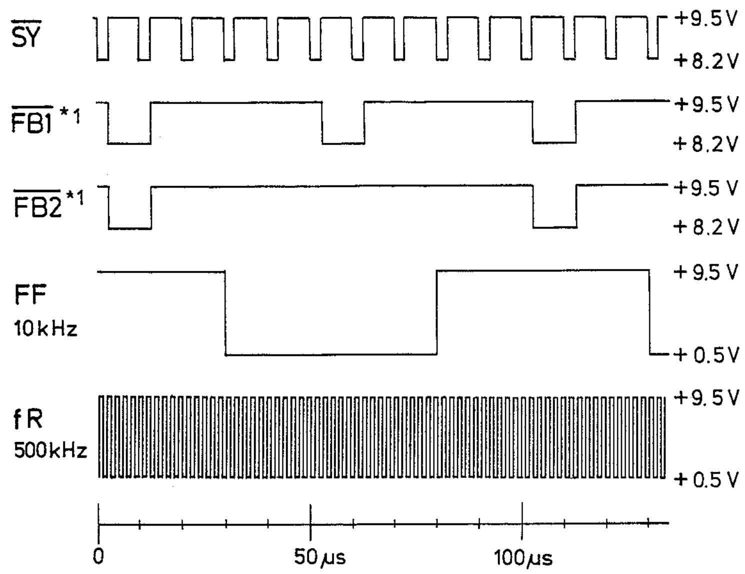
VCO Conversion Gain (Ko)
The conversion factor between VCO frequency and control voltage in radians/second/volt.

Phase Detector Gain Factor (Kd)
The conversion factor between the phase detector output voltage and the phase difference between input and VCO signals in volts/radian. At low input signal amplitudes, the gain is also a function of input level.



3.5.3. Programmable divider and Phase-locked loop

The programmable divider comprises divider 1, HEF 4751, pos. 301/U2, and two prescalers 303, 305, RF-U2, assisted by flip-flop 304. The operation of these fast prescalers is based on the 'pulse swallow' principle, see appendix. They are switched between division factor 10 and 11 by the signals $\overline{FB1}$ and $\overline{FB2}$, whereby $\overline{SY}$ acts as synchronizing signal.



*1 The feedback signals $\overline{FB1}$ and $\overline{FB2}$ to the prescaler/ RF-U2 are dependent on the selected RF frequency: 100 kHz, 10 kHz and 1 kHz = or ≠ 0, see table, e.g. frequency setting 340.xxx MHz.

Freq. (MHz)	$\overline{FB1}$	$\overline{FB2}$	$\overline{SY}$
340.000	–	–	⊔⊓⊔
340.100	–	⊔⊓⊔	⊔⊓⊔
340.01x	⊔⊓⊔	–	⊔⊓⊔
340.11x	⊔⊓⊔	⊔⊓⊔	⊔⊓⊔

Fig. 8 Unit 2, Timing diagram HEF 4751, selected frequency 340.119 MHz

The division factor N is set between 50.000 and 220.000 by the 6 prog. inputs $\overline{A0}$ ... $\overline{A3}$, $\overline{B2}$, $\overline{B3}$ in BCD code in a bit parallel, digit-serial format. Divider 1 provides a fast output signal FF at output 27, which can have a phase jitter of ±1 system input period, to allow fast frequency locking. The slow output signal FS at output 25, which is jitterfree, is used for fine phase control at a lower speed.

The 5 MHz X-tal frequency is divided by the internal divider –set to 500 : 1 at the prog. inputs – to the fast 10 kHz reference frequency. The outputs PC 1 ('fine' / analog phase comparator output) and PC2 ('coarse' / digital phase comparator output) are coupled to an active low-pass filter 315/RF-U2. For improved reaction time two speed-up capacitors are inserted into the low-pass section. The maximum control speed at the outputs is 0.1 V/ms.

3.5.4. Level control, fine and coarse attenuation

The output signal of the main oscillator VCO 1 is fed to the automatic level control, where the RF level is adjusted to -1 dBm ±1 dB at mixer 851, pin 4. The RF signal is detected by diode 410 and applied to amplifiers 302/301. The dc voltage at 301.6 (about 4.5 V ±0.2 V) controls pin diodes 411, 412, 413.
Amplitude/video modulation can be added after this stage. The appropriate signal is applied from unit 3 to mixer 851, pin 2.

The final section provides fine and coarse attenuation in two programmable stages. Fine adjustment is carried out by the pin diode attenuator on RF-unit 1, providing a continuous range from 0 to 20 dB in 1 dB steps. Additional temperature compensation is realized by NTC resistor 740.
Coarse adjustment is achieved by a 100 dB attenuator in 10 dB steps at the RF output. The 0 to 9 dB range of the pin diode attenuator is used for level setting from -7 dBm to -117 dBm (PM 5390 S: +13 dBm to -117 dBm), while the 10 to 20 dB range is active from -117 to -127 dBm only.

The circuit diagram of the pin diode attenuator and the applied control voltage VR 2 (exponential characteristic) is shown in fig. 9a PIN diodes have a resistance characteristic for HF signals. The value of the HF resistance depends on the dc bias current. For adjustment procedure the characteristic of the control voltage VR 2 may be changed by solder joint E on unit 1.

Complete control of the coarse and fine attenuation is achieved by output lines B7, C0 – C7 of port 2 and B0 - B2, port 3, on control unit 2.

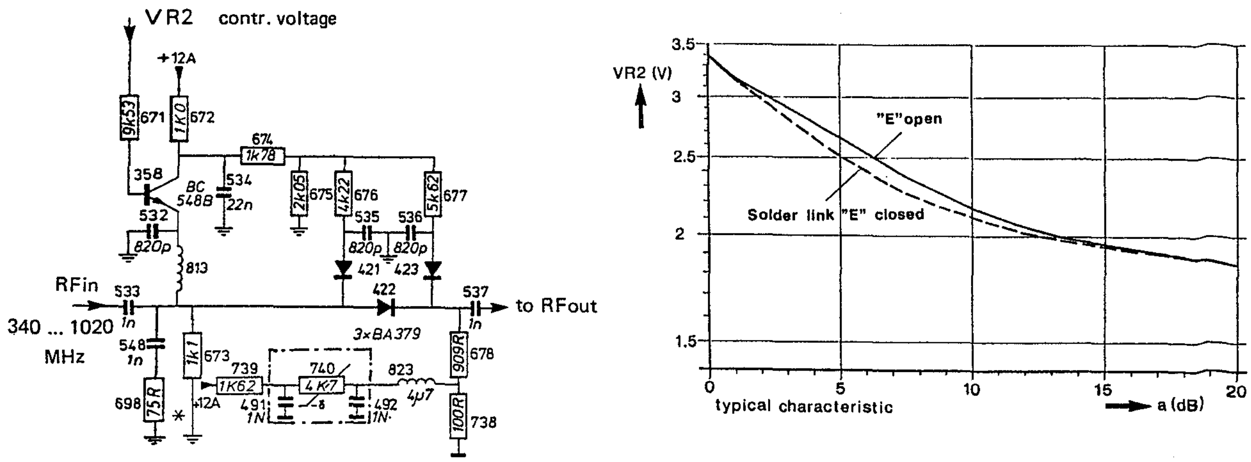


Fig. 9a RF-unit 1, pin diode attenuator

Level RF OUT dBm	PM 5390 10 dB	20 dB	30 dB	40 dB	PM 5390S (software I-9.1/II-9.1) 10 dB	20 dB	30 dB	40 dB	PM 5390S (software I-A.1/II-A.1) 10 dB	20 dB	30 dB	40 dB
+13 ... +3	not possible				–	–	–	–	–	–	–	–
+3 ... -6	not possible				x				x			
-7 ... -16	–	–	–	–		x				x		
-17 ... -26	x						x		x			
-27 ... -36		x				x				x		
-37 ... -46			x				x				x	
-47 ... -56				x				x				x
-57 ... -66	x			x	x			x	x			x
-67 ... -76		x		x		x		x		x		x
-77 ... -86			x	x			x	x			x	x
-87 ... -96	x		x	x	x		x	x	x		x	x
-97 ... -106		x	x	x		x	x	x		x	x	x
-107 ... -127	x	x	x	x	x	x	x	x	x	x	x	x

Fig. 9b Coarse attenuator setting

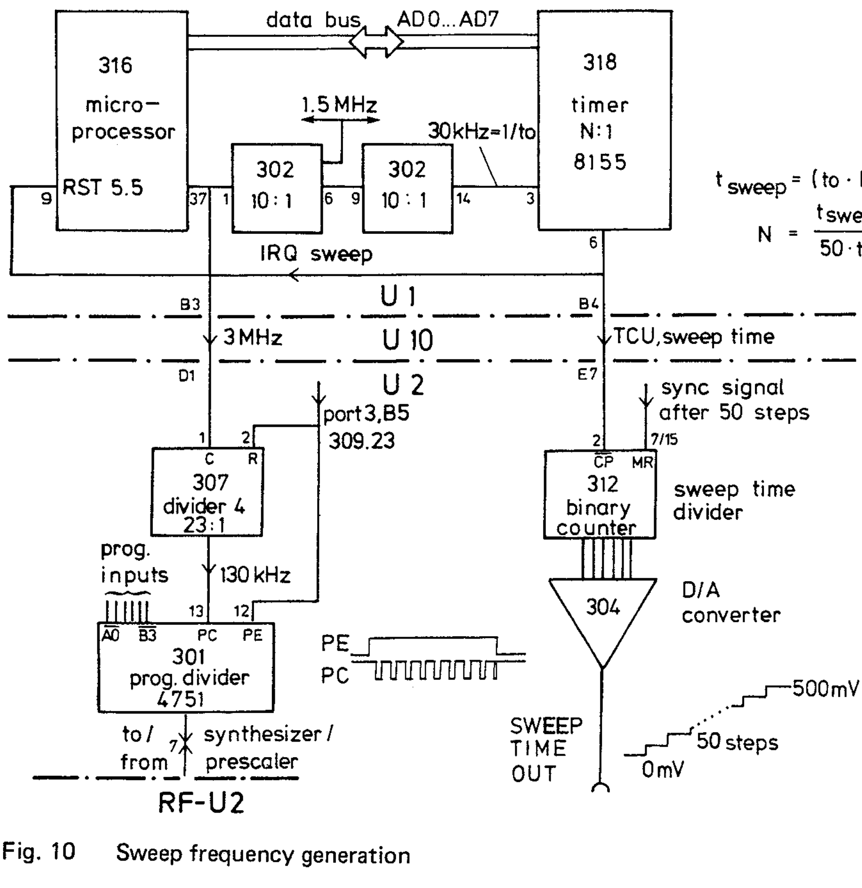
3.5.5. Sweep frequency generation

As mentioned the frequency of the main oscillator is set by the programmable divider in the main PLL system (unit 2). A sweep is generated by stepwise changing the division factor: in equal time distances (t_{sweep}/50) the division factor is increased by a constant calculated value and read-in. The increase of the factor can be 1 ... 1000, corresponding to frequency changing of (1 ... 1000) x 1 kHz per step.

A start pulse IRQ sweep for setting the next division factor of the PLL loop is sent to the interrupt input RST 5.5 of the microprocessor. The processor counts 50 pulses and resets the system.
The input sequence for reading the division factor into the prog. counter is controlled at input PC by the 3 MHz processor clock divided to 130 kHz by the 23 : 1 divider 4, IC 307 / U2. Program enable, PE, starts the process. Taking the processor clock assures a synchronous handling of the division factor with PE and PC.

The figure below also shows the generation of the sweep time. The set sweep time is converted by the processor into a division factor N of the timer circuit within IC 318 /U1. At each setting of a new frequency (IRQ sweep, see above) the TCU signal increases the state of the binary counter 312/U2 by 1. 6 output lines are connected to the summing point of the operational amplifier 304 via resistors 643 - 648, the values of which are binary weighted. So the output of IC 304 shows a staircase signal. The output is connected to the SWEEP TIME OUT socket at the rear of the instrument, where a staircase voltage from 0 to 500 mV in 50 steps of 10 mV each is available; the period of the staircase ramp, i.e. the sweep time, to which 200 ms fly-back time must be added, can be set from 0.05 s to 20 s.

The IRQ sweep pulses are counted, see above, and after 50 steps a sync signal is sent as reset signal to the binary counter 312. This signal has a duration of 200 ms which is equal to the fly-back time during which setting to the start frequency and settling of the PLL system is achieved. The reset signal, input 312.7/15 as the sync pulse, is used for master clear after power-on.



$$t_{sweep} = (to \cdot N) \cdot 50$$

$$N = \frac{t_{sweep}}{50 \cdot to} = 600 \cdot t_{sweep}$$

Fig. 10 Sweep frequency generation

3.6. POWER AMPLIFIER; RF–UNIT 12 (PM 5390 S), fig. 47

The instrument version PM 5390 S supplies increased output level up to +13 dBm, corresponding to an output voltage of 1 Vrms into 50 Ω.
There does not exist any conversion kit to change PM 5390 into PM 5390 S.

The 20 dB power amplifier has two signal paths:
During output level settings between -127 dBm and -17 dBm (software version I-A.1/II-A.1) the power amplifier is supplied by -12 V, instruments including software I-9.1/II-9.1 between -127 dBm and -27 dBm. In this case pin-diodes 402, 404 have low resistance, while pin-diodes 401, 403 have high resistance. The RF signal passes to amplifier 304, where insertion loss of 2 dB is compensated. Frequency response is adjusted by C517 and R620.
If output levels > -17 dBm (software I-9.1/II-9.1 > -27 dBm) are selected the power amplifier is supplied by +24 V. The signal path is switched over and the RF is fed to the 20 dB amplifier stage comprising amplifiers 301, 302 and 303. The frequency response of this signal path is adjusted by C520 and R622, see table 7.3.1, final adjustments.

For soldering of replacement components use only resin-core solder tin with silver.

3.7. POWER SUPPLY; UNIT 10 (motherboard)

Seven supply voltages are generated by the supply section of unit 10:
Two stabilized +5 V voltages are generated by regulators 354/355, +5A for the digital part of the units 1, 2, 3, 10 and +5B for the keyboard/display interface, units 4 and 5. The display unit is separately supplied in order to have less influence by scan interference.

+12A is a stabilized voltage realized by the four-terminal voltage regulator 351; it supplies RF units 1 and 2. Ground connections are conducted separately to U10 to have less interference/hum and should not be altered.
Special effort is made for the supply voltage of the loop filter in the PLL circuitry: a +35 V stabilized supply voltage is generated by precision regulator 302 on unit 7. This voltage is applied via coaxial cable to RF-unit 2, where additional filtering and hum suppression is achieved. Overmore this voltage is applied to precision regulator 323 on RF–U2 to generate +27 V supply voltage for the loop filter 315.

Two regulators, 352, 353, generate three supply voltages, +12 B and -12 A/-12 B, for units 2, 3 and 10.

Some other stabilized voltages are generated directly on the units where they are needed:

- regulator 322, RF-U2, generates +5 V,
  regulator 321, RF-U2, supplies ECL voltage for the prescaler
- regulator 307, RF-U1, generates +5 V.

Furthermore control voltages to switch the RF units 1 and 2 are realized by 8 reed relais 801-808 and inverter 356.

+24 V supply voltage and reed relay 810 are present only in the PM 5390 S version to supply and switch the 20 dB power amplifier.

4. ACCESS TO PARTS

4.1. DISMANTLING THE INSTRUMENT

- Unplug the mains connector
- Fold up the handle to the top. For this push the buttons of the handle
- Loosen the 4 screws at the rear
- Dismantle the cabinet

4.2. FUSE, MAINS TRANSFORMER

For mains voltage setting and fuses and the assigned safety instruction see the operating manual PM 5390, chapter 2.2.3 and 2.3.

4.3. CARRYING HANDLE

- Prise off the centre knobs from each pivot, using a screwdriver in one of the small slots at the sides of the knobs.
- Remove the cross-head screws that are now accessible.
- Bend both arms of the handle slightly outwards and take it off the cabinet.
- Grip and arms of the carrying handle must be ordered separately (see mechanical parts list).
  A complete carrying handle can easily be constructed by pressing the arms into the grip.

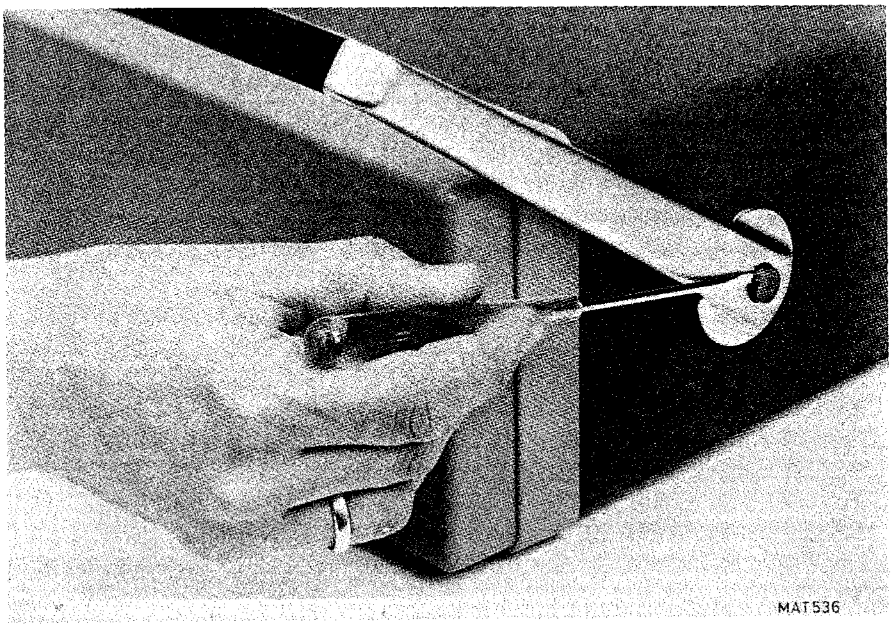


Fig. 11 Removing the carrying handle

4.4. PUSHBUTTONS

For changing knobs for pushbuttons it is necessary to open the cabinet and remove unit 5, see 4.6.

4.5. 'RF OUTPUT' CONNECTOR

- Remove the cabinet, see 4.1.
- Remove the plastic cover of the mains switch
- The textplate can now carefully be removed (it is fitted by double-sided adhesive tape).
- Remove the RF output connector piece from the progr. attenuator by a spanner 8 mm (PM 5390S: from PA stage 815).
- Remove four countersunk screws M 2.5 of the RF OUTPUT connector
- For replacement of the BNC connector unsolder from semi-rigid cable

4.6. UNIT 4, 5; KEYBOARD/DISPLAY UNIT

- Remove the cabinet, see 4.1
- Remove the plastic cover of the mains switch
- The textplate can now carefully be removed (it is fitted by double-sided adhesive tape).
- Remove the RF output connector piece, see 4.5.
- Remove the four screws in the corners of the front plate (cross headed screws).
- Remove front plate and front frame with the printed card boards U4 and U5. Be careful when the complete unit is removed from the 29 pole CIS-connector of unit 10.
- For demounting the keyboard/display interface U4, remove 4 screws M2.5, which are visible at the wired side of the pcb.
- Now unit 4 is only held with two CIS-connectors to the frontplate with the keyboard/display U5.
- Pull out the pcb U4; all parts of this card are now accessible.
- For demounting pcb U5 remove six countersunk screws M2.5 of the front plate.

4.7. RF–UNITS

- Dismantle the instrument, see 4.1.
- Remove the screening plate fixed to mains transformer and RF case.
- Loosen the retaining clips of the IEC-bus adapter, unit 6, and remove flat cable connection to the CPU/U1
- Remove unit 1 (attention for short circuit of the NiCd battery, when pcb is removed)
- Remove the connectors S1 and S2 of unit 2
- Remove unit 2 and unit 3
- Unsolder the coax cables LP1, LP2/LP3 of unit 2
- Unsolder the coax cable, point 23 of unit 3
- Remove the RF output connector piece 854 from progr. attenuator, loosen nut by spanner 8 mm (PM 5390S from PA stage 815).
- Replug the RF connector 'fR' of RF/unit 1
- Remove the RF output connector piece 883, loosen nut by spanner 8 mm
- Unsolder all connections to the motherboard of the RF unit except coax cables (see table"solder connections", fig. 42).
- Loosen the two junction plates and the ground connection between RF case and unit 10 (bottom side)
- Remove the 4 countersunk screws M4 at the right side wall.
- Remove the complete RF case incl. attenuator (PM 5390S: incl. power amplifier)
- Remove all screws (8 x M2.5) of the cover plate of RF case and take it off
- Remove twelve screws M 2.5 of the RF-motherboard
- Remove the RF motherboard incl. RF-unit 1 and RF-unit 2 of the RF case
- Remove the 4 screws of RF motherboard
- unit RF-U1 and RF-U2 can now be removed from the CIS-connectors of the RF motherboard.

Access to RF-U1/U2

- pull down the upper screening cover a little bit and hook off three spring shackles at one side and remove the cover.
- all four covers can be removed in the same way. All components of pcbs are now accessible.

For all checks and adjustments the complete RF units must be closed and the specified warm-up time must be finished.

Attention: When RF-U1 and RF-U2 are assembled again, special care must be taken: the inside screening mats of the cover may not dip (the covers must be slidely movable).

5. PERFORMANCE CHECK

5.1. GENERAL INFORMATION

WARNING:
Before switching on, ensure that the instrument has been installed in accordance with the instructions outlined in Section 2 of the Operating Manual: Installation instructions.

This procedure is intended to:
- check the instrument's specification
- be used for incoming inspection to determine the acceptability of newly-purchased instruments and/or recently-recalibrated instruments.
- check the necessity of recalibration after the recommended recalibration interval of 1 year.

ATTENTION:
The procedure does not check every detail of the instrument's calibration; rather, it is concerned primarily with those parts of the instrument which are essential to measurement accuracy and correct operation. Removing the instrument covers is not necessary to perform this procedure. All checks are made from the front panel.

If this test is started within a short period after switching on, bear in mind that steps may be out of specification, due to insufficient warming-up time. To avoid this situation, allow the specified warming-up time of 30 min.

5.2. GENERAL FUNCTIONAL TEST

Immediately after power being switched on a selftest routine is performed under which ROM and RAM are tested. If a fault is detected a single numeric digit in the first place of the frequency field on the display indicates the location of the fault. The rest of the display remains dark. The numeric digits are assigned to the memories as follows.
1 ROM
2 RAM
3 CMOS–RAM

After this all segments and decimal points of the display and all LEDs –only the 'REMOTE' LED excepted– are switched on for about 3 seconds for testing.

When the selftest routine is terminated, the display will show its initial reading:

000.000 MHz	0.000 MHz	.00 s	-127 dBm ⊗
FREQUENCY	ΔFREQUENCY	SWEEP TIME	LEVEL

For further information see chapter 6.1. Error Messages.

Set the instrument to 1 MHz output frequency, -7 dBm output level; check the signal by means of an oscilloscope.

Set the step attenuation to -8 dBm and -17 dBm and check the output signal.

Perform frequency sweep from 10 MHz to 15 MHz (ΔFREQUENCY = 5 MHz), sweep time 0.50 s; check the output signal by means of an oscilloscope.

Perform TV signal: set the instrument to 175.25 MHz, output level to -27 dBm, modulation VIDEO/INT.FM; apply external CVBS signal to the VIDEO input.
Check the TV signal by means of CTV receiver at VHF channel 5 (E5).

6. SELF–TEST PROGRAM, DIAGNOSTIC PROGRAM

6.1. SELF–TEST PROGRAM, ERROR MESSAGES

A self-test routine is part of the normal program.
Malfunctions of the central processing unit of the PM 5390 are traced internally. An error message is output by displaying one numeric digit 1 ... 4 at the first position of the frequency display field, all other elements of the display being blanked.
Error localization of the CPU:

Displayed numeral	localization of malfunction
1	EPROM, System program
2	RAM, Working memory
3	CMOS–RAM, Data memory
4	TIMER, Central timing control

6.2. TEST–PROM, DIAGNOSTIC PROGRAM

For simple fault finding in the digital circuitries of PM 5390 and PM 5390S several test programs can be realized by means of a special test PROM.
Moreover faults may be detected by other or conventional methods.
Generally the voltages of the power supply should be checked at first (see table checks and adjustments). While the self-test routine is part of the normal program, the diagnostic program must be activated by replacing the built-in program memory IC311/unit 1 of the CPU by the test PROM PM 5390 (see fig. 43). The instrument must be disconnected from the mains before. The PROM must properly be inserted in the correct direction – pins all in and not bent. The test PROM PM 5390 should be ordered directly via PHILIPS Supply Centre Service, Hamburg; it has no service code number.
After POWER ON 2 zeroes '00' must be visable in the 2 leftmost positions of the frequency display field. If '88' is flashing instead the initial check has detected a RAM failure within IC 318, unit 1. Correct '00' display allows the following test programs to be selected:

1. Keyboard test
Keying-in 01 effects display '01' in the 1st and 2nd position of the frequency display field. The codes of the subsequent pushbutton actions are decimally displayed in the level display field; for the codes see fig. 12. After all keys have been pushed, the LEDs 'SINGLE' and 'CONT' are lit. Now the program can be left by successively pushing 'CONT', 'SINGLE'. After pushing 'CONT' the LED 'CONT' turns off; if after this a different key instead of 'SINGLE' is pushed, 'CONT' lightens again.

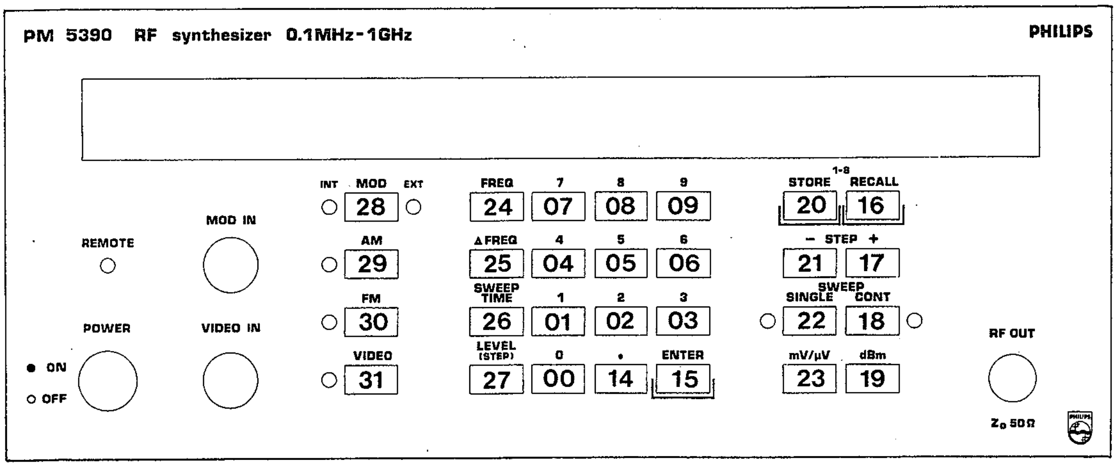


Fig. 12 Keyboard code

2. Display test

Key in: 02; display: '02'.

All seven-segment digits and LEDs (except 'REMOTE') are lightened. By pushing any key except 'ENTER' they are switched off and on.

'ENTER' switches to the next part of this test:

- all displays show 0, 1, 2, ... 9.
- an '8' is passing from the leftmost to the rightmost display position.
- all display segments ('8') and decimal points are flashing.

Pushing any key ends this test:

- a decimal point passes from the left of the display to the right.

The initial display '00' appears on the 2 leftmost positions of the frequency display field.

3. RAM test

Key in: 03; display: '03'.

This test checks the CMOS–RAM (data memory), IC 313, unit 1, and the RAM section within IC 318, 8155. The test duration is ca. 7 s. If no failure is detected '00' is displayed, see above.

Error indication:

1st position	: c ≙ CMOS–RAM, IC 313 1 ≙ 8155 RAM, IC 318	
4th – 6th position:	address within the IC	(decimal)
7th – 9th position:	written data	(decimal)
10th – 12th position:	read data	(decimal)

4. Port test

Key in: 04; display: '04'.

All output ports are set to high level: unit 1, IC 318, pins 21 - 35 and unit 2, ICs 305/309, pins 1-4, 10 - 25, 37 - 40.

Pushing any key except 'ENTER' effects alternating low and high level at all ports.

During high level the LEDs MOD INT/EXT, AM, SWEEP SINGLE/CONT are lighting, LEDs FM and VIDEO are flashing simultaneously.

'ENTER' ends the test.

5. IEEE/IEC bus test

The test is activated by addressing the instrument via the IEC bus.

After addressing the 'REMOTE' LED is lit. The numerical digits sent after this are displayed on the 10 first display positions. If more digits are sent they will overwrite the preceding digits starting at the left position. Only numerical digits are accepted, other characters are ignored.

After reception of DCL (Device Clear) or SDC (Selective Device Clear) 'ccccccc' is displayed.

Example for a small IEC bus test routine using hp-85 controller:

```
10 RESET 7
20 REMOTE 704
30 OUTPUT 704;"1234567890"
40 PAUSE
50 OUTPUT 704;"0000000000"
60 PAUSE
70 CLEAR 704
80 PAUSE
90 OUTPUT 704;"6666666666"
100 PAUSE
110 LOCAL 704
120 PAUSE
130 GOTO 20
```

7. CHECKING AND ADJUSTING

7.1. GENERAL INFORMATION

The following information provides the complete checking and adjusting procedure for the instrument. As various control functions are interdependent, a certain order of adjustment is often necessary. The procedure is, therefore, presented in a sequence which is best suited to this order, cross-reference being made to any circuit which may affect a particular adjustment.
Before any check, the instrument must attain its normal operating temperature.

- Warming-up time under average conditions is 30 minutes.
- Adjustments should be made after 60 minutes
- Ambient temperature (23 ±1)°C
- Mains voltage, nominal values ±10 %
- The cabinet must be closed and should be removed only for a short time for adjustment.
- Where possible, instrument performance should be checked before an adjustment is made.
- All limits and tolerances given in this chapter are calibration guides, and should not be interpreted as instrument specifications unless they are also published in chapter 1.2. of the Operating Manual.
- Tolerances given are for the instrument under test and do not include test equipment error.
- If not explicitely stated otherwise, the voltage potentials refer to the relevant contact measured against measuring earth (⊥).

7.2. RECOMMENDED TEST EQUIPMENT

- The following abbreviations are used for settings and for the test equipments:

X	≙ selected parameter mode or input
↧	≙ keep setting concerned
–	≙ parameter not used
o–	≙ output not terminated
●–	≙ output, terminated with 50 Ω, e. g. HP 10100C
●– 20 dB	≙ attenuator 20 dB/50 Ω, e. g. Midwest microwave 313
Vac, Vdc	≙ Digital multimeter for a. c. and d. c. measurement, e. g. PM 2534
OSC	≙ Oscilloscope 100 MHz e. g. PM 3267
C/T	≙ Counter/Timer e. g. PM 6665/421
SPA	≙ Spectrum analyzer 1 GHz e. g. TR 4132 SPA setting: BW ≙ bandwidth, SW ≙ scan width, ST ≙ scan time
FAM *	≙ Modulation analyzer e. g. R&S FAM/B2/B8
PMTR *	≙ Power meter 1 GHz e. g. HP 436A + Sensor 8482 A or R&S URV5 + URV5–Z2
CTV	≙ CTV-receiver
CTVS	≙ PAL pattern generator e. g. PM 5515
SV	≙ RF-millivoltmeter R&S URV5

* Instead of single instruments Modulation analyzer and Power meter a Modulation analyzer HP 8901 B, which includes a Power meter, is available; range 150 kHz - 1300 MHz; Power sensor 11722 A.

For units 1, 2, 3 **extension boards** are available, to be ordered directly via Supply Centre Service Hamburg; they have no service code number.
For the **test PROM** see chapter 6.2.

On the next page you find a conversion table for dBm/voltage values; this table you can also find in the operating manual, fig. 33.

dBm	Volt	dBm	Volt	dBm	Volt
-127	0.1 µV	-73	50 µV	-19	25 mV
-126	0.11 µV	-72	56 µV	-18	28 mV
-125	0.13 µV	-71	63 µV	-17	32 mV
-124	0.14 µV	-70	71 µV	-16	35 mV
-123	0.16 µV	-69	79 µV	-15	40 mV
-122	0.18 µV	-68	89 µV	-14	45 mV
-121	0.20 µV	-67	100 µV	-13	50 mV
-120	0.22 µV	-66	112 µV	-12	56 mV
-119	0.25 µV	-65	126 µV	-11	63 mV
-118	0.28 µV	-64	141 µV	-10	71 mV
-117	0.32 µV	-63	158 µV	- 9	79 mV
-116	0.35 µV	-62	178 µV	- 8	89 mV
-115	0.40 µV	-61	199 µV	- 7	100 mV
-114	0.45 µV	-60	0.22 mV	- 6	112 mV *
-113	0.50 µV	-59	0.25 mV	- 5	126 mV
-112	0.56 µV	-58	0.28 mV	- 4	141 mV
-111	0.63 µV	-57	0.32 mV	- 3	158 mV
-110	0.71 µV	-56	0.35 mV	- 2	178 mV
-109	0.79 µV	-55	0.40 mV	- 1	199 mV
-108	0.89 µV	-54	0.45 mV	0	.22 V
-107	1.00 µV	-53	0.50 mV	+ 1	.25 V
-106	1.12 µV	-52	0.56 mV	+ 2	.28 V
-105	1.26 µV	-51	0.63 mV	+ 3	.32 V
-104	1.41 µV	-50	0.71 mV	+ 4	.35 V
-103	1.58 µV	-49	0.79 mV	+ 5	.40 V
-102	1.78 µV	-48	0.89 mV	+ 6	.45 V
-101	1.99 µV	-47	1.00 mV	+ 7	.50 V
-100	2.2 µV	-46	1.12 mV	+ 8	.56 V
-99	2.5 µV	-45	1.26 mV	+ 9	.63 V
-98	2.8 µV	-44	1.41 mV	+10	.71 V
-97	3.2 µV	-43	1.58 mV	+11	.79 V
-96	3.5 µV	-42	1.78 mV	+12	.89 V
-95	4.0 µV	-41	1.99 mV	+13	1.00 V *
-94	4.5 µV	-40	2.2 mV		
-93	5.0 µV	-39	2.5 mV		
-92	5.6 µV	-38	2.8 mV		
-91	6.3 µV	-37	3.2 mV		
-90	7.1 µV	-36	3.5 mV		
-89	7.9 µV	-35	4.0 mV		
-88	8.9 µV	-34	4.5 mV		
-87	10.0 µV	-33	5.0 mV		
-86	11.2 µV	-32	5.6 mV		
-85	12.6 µV	-31	6.3 mV		
-84	14.1 µV	-30	7.1 mV		
-83	15.8 µV	-29	7.9 mV		
-82	17.8 µV	-28	8.9 mV		
-81	19.9 µV	-27	10.0 mV		
-80	22 µV	-26	11.2 mV		
-79	25 µV	-25	12.6 mV		
-78	28 µV	-24	14.1 mV		
-77	32 µV	-23	15.8 mV		
-76	35 µV	-22	17.8 mV		
-75	40 µV	-21	19.9 mV		
-74	45 µV	-20	22 mV		

* PM 5390 S only

Fig. 13
RF output level (into 50 Ω): table of dBm/voltage values
HF-Ausgangspegel (Zo = 50Ω): dBm-/Spannungstabelle
Niveau du sortie HF (Zo = 50 Ω): table des valeurs dBm/voltage

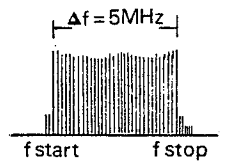
7.3. Table of checks and adjustments

7.3.1. Final adjustment, complete instrument

Seq.	Keyboard operation FREQ MHz	ΔFREQ MHz	SWEEP TIME (s)	LEVEL dBm	mV/µV/V	MODULATION INT EXT	AM	FM	VIDEO	±STEP freq.	level	SWEEP SINGLE	CONT	STORE	RECALL	measured via: outputs SWEEP T. OUT	RF OUT	test point	measuring instrument (see 7.2.)	measured value	max.hum	adjustment control position	remarks general: for the correct sequence of pushbutton actions see operating manual
																		line		44W(53W)			power consumption PM 5390 (PM 5390S)
1.1.																		P3/U7	Vdc/Vac	35±1.0V	<5mVpp		power supply
1.2.																		+5A	Vdc/Vac	5.0±0.25V	<10mVpp		
1.3.																		+5B	Vdc/Vac	5.0±0.25V	<10Vpp		
1.4.																		+12A	Vdc/Vac	12.0±0.1V	<2mVpp	609	
1.5.																		+12B	Vdc7Vac	12.0±0.25V	<2mVpp		
1.6.																		-12A	Vdc/Vac	-12.0±0.25V	<2mVpp		
1.7.																		-12B	Vdc/Vac	-12.0±0.25V	<2mVpp		
1.8.																		+24	Vdc/Vac	+24±1.2V	<10mVpp		only PM 5390S
1.9.																							
																							Keyboard operation
2																							display indication after POWER ON
2.1.	000.000	0.000	.00	-127⊗																			Δf = 7.900 when ENTER key pressed
2.2.	123456	7.890	.12	-34 ⊗																			flashing frequency display when ENTER key pressed.
2.3.	1020.	7.900	.12	-34 ⊗																			For incorrect input keying and exceeding ranges see operating manual, chapt. 3.4.9.
2.4.	(123.456	7.900	.12	-34⊗)											x								stacked command; key in: FREQ, RECALL, ENTER
2.5.	111.	-	-											x1									store parameter: key in: data, STORE 1...3
2.6.	222.													x2									
2.7.	333.													x3									
2.8.	111.000														x1								recall memory; key in: RECALL 1...3
2.9.	222.000														x2								
2.10.	333.000														x3								
2.11.	45.	90.	00							+x													frequency step; key in: data, ENTER, +STEP 10x
2.12.	945.000	↓	↓							+x													last step (11.step impossible)
2.13.	945...45									-x													frequency step; key in: -STEP 10x (11. step impossible)
2.14.						- x -																	modulation, key in: MOD INT/EXT (no reaction)
2.15.						x or x	x																mod. AM, key in: AM, MOD INT/EXT (push 2x)
2.16.						- -	x																mod. off, key in: AM (all LEDs off)
2.17.						x or x		x															mod. off, key in: FM, MOD INT/EXT (push 2x)
2.18.						- -		x															mod. FM off, key in: FM (all LEDs off)
2.19.	29.								x														Video, flashing LED VIDEO
2.20.	30.					x or x	x		x														Video AM, key in: Video, AM, MOD INT/EXT (push 2x
2.21.	↓					x or x		x	x														Video FM, key in: VIDEO, FM, MOD INT/EXT (push 2x
2.22.						- -			x														Video off, key in: VIDEO (all LEDs off)
2.23.	10.	5.000	0.50									x											single sweep, key in: data, ENTER, SINGLE (LED SINGLE 1 flash)
2.24.	10.	5.000	0.50										x										cont. sweep, running sweep interrupt by CONT
2.25.				xx ⊗..⊗..⊗																			LEDs level PM 5390, key in: LEVEL, dBm, mV/µV (push 2x)
2.26.				xx± ⊗..⊗..⊗..⊗																			LEDs level PM 5390S, key in: LEVEL, ±dBm (2x), mV/µV/V (3x)

Seq.	Keyboard operation FREQ MHz	ΔFREQ MHz	SWEEP TIME (s)	LEVEL dBm	mV/µV/V	MODULATION INT	EXT	AM	FM	VIDEO	±STEP freq.	level	SWEEP SINGLE CONT	STORE	measured via: outputs SWEEP T. OUT	RF OUT	test point	measuring instrument (see 7.2.)	measured value	adjustment, control position	remarks general: for the correct sequence of pushbutton actions see operating manual
3.																					Frequency, C/T setting: gate time 1s
3.1.	1000.			-7 ⊗												●–		C/T	1000MHz±1kHz	RF-U2/C563	time base, adjustment after 80 min.
3.2.	10...1000	90.0		-7 ⊗							+x					●–		↓	10MHz...1GHz±1×10^{-6}		frequency steps: 10,100,190,280,370,460,550 MHz, 640,730,820,910 and 1000 MHz
3.3.	100.	.001		-7 ⊗							+x					●–		↓	100.001MHz±100Hz		frequency step-up 1kHz
3.4.	↓	.001		-7 ⊗							-x					●–		↓	99.999MHz±100Hz		frequency step-down 1kHz
3.5.	↓	.010		-7 ⊗							+x					●–		↓	100.010MHz±100Hz		frequency step-up 10kHz
3.6.	↓	.010		-7 ⊗							-x					●–		↓	99.999MHz±100Hz		frequency step-down 10kHz
3.7.	.100			-7 ⊗												●–		OSC/CT	100kHz±1Hz		symmetr. waveform; C/T setting: gate time 10s
4.																					Output level, coarse attenuator
4.1.	0.1...19.1	1.000		-7 ⊗							+x					●–		PMTR	-7dBm±2dB	RF-U1/R638	setting error incl. frequency response, adjustment range ≤ 0.5 dB
4.2.	19.1...1019.1	10.0		-7 ⊗							+x					●–		↓	-7dBm±2dB		if necessary, iterate seq. 4.1.
4.3.	0.1...19.1	1.000		+13 ⊗							+x					●–		↓	+13dBm±2dB	RF-U1/R638	setting error incl. frequency response PM5390S, adjustment range ≤ 0.5 dB
4.4.	19.99...679.99	10.00		+13 ⊗							+x					●–		↓	+13dBm±2dB	and	
4.5.	680...1019.99	10.00		+13 ⊗							+x					●–		↓	+13dBm±3dB	RF-U12/R622 /C520	C520/RF-U12 additional f > 850 MHz
4.6.	470.			-7 ⊗												●–		↓	-7dBm±2dB*[1]		*1 use for reference value seq. 4.7. - 4.9.
4.7.	↓			-17 ⊗												●–		↓	ref*[1](-10±0.3)dBm		coarse attenuator setting (10 dB steps)
4.8.	↓			-27 ⊗												●–		↓	ref*[1](-20±0.3)dBm		
4.9.	↓			-37...-57 ⊗												●–		SPA/*			*, or other UHF equipment
5.																					Fine attenuator setting, remove plug S2/unit 2 (coarse attenuator ≙ 100 dBm not active)
5.1.	470.			-107 ⊗		–	–	–	–	–						●–	LP1/U2	PMTR Vdc	-7dBm±2dB *[2] 3.4V±50mV		*2 use for reference seq. 5.2. - 5.5. add. information , test pt. LP1/U2 or RF-U1/VR2
5.2.	↓			-116 ⊗												●–		PMTR	ref*[2]-9dBm±0.1dB	R681/U2 and R662/U2 } *3	pin diode attenuator
5.3.	↓			-107...-117								-x				●–		↓	ref*[2]0...-10dBm±0.3dB		push -STEP button for single 1dB steps
5.4.	↓			-118...-122								-x				●–		↓	ref*[2]-11...-15dBm±0.8dB		if necessary, iterate 5.2/5.3.
5.5.	↓			-123...-127								-x				●–		↓	ref*[2]-16...-20dBm±2dB		*3 if tolerance exceeds close solder joint "E"/U1 repeat seq. 5.2. to 5.4. (software I-A.1/II-A.1) plug in S2/unit 2 when adjustment is finished
5.6.	470. 0.1/250/850/ 1000			-26 ⊗ -27 ⊗												●– ●–		SV/* ↓	ref*[4] ref*[4]-1dBm±0.8dB	RF-U12 C517/R620	PM 5390S (software version I-9.1/II-9.1) *[4] use for reference , *other RF equipment next step -26 dBm to -27 dBm
5.7.	470. 0.1/250/850/ 1000			-17 ⊗ -17 ⊗												●– ●–		PMTR ↓	ref*[4] ref*[4]-1dBm±0.8dB	RF-U12 C517/R620	PM 5390S (software version I-A.1/II-A.1) *[4]use for reference next step down -16dBm to -17dBm
5.8.	101.			-127 ⊗		–	–	–	–	–						●–			-127dBm±3dB		check, if RF equipment available

Seq.	Keyboard operation FREQ MHz	FREQ MHz	SWEEP TIME (s)	LEVEL dBm	mV/µV/V	MODULATION INT	EXT	AM	FM	VIDEO	REMOTE contr.	measured via: inputs MOD IN	VIDEO IN	outputs SWEEP T. OUT	RF OUT	test point	measuring instrument (see 7.2.)	measured value	adjustment, control position	remarks general: for the correct sequence of pushbutton actions see operating manual.
6.																				Spectral purity checks neces. after repaired RF-units
6.1.	0.1...510			-7 ⊗		—	—	—	—	—					●—		SPA	< -30dBc		harmonics PM 5390 — advised SPA setting:
6.2.				0 ⊗		—	—	—	—	—					●—		SPA	< -30dBc		harmonics PM 5390S — BW=300kHz, SW=100MHz, ST=5ms
6.3.				+7 ⊗		—	—	—	—	—					●—		SPA	< -25dBc		
6.4.				+13 ⊗		—	—	—	—	—					●—		SPA	< -20dBc		
6.5.	0.1...339.99			-7 ⊗		—	—	—	—	—					●—		SPA	< -30dBc		non harmonics; select some frequencies
6.6.	340...1019.99					—	—	—	—	—					●—		SPA	< -40dBc		
6.7.	5...1019.99					—	—	—	—	—					●—		FAM	< 100Hz/rms		residual FM; FAM setting: FM, RMS, filter 0.3/3kHz, select some freq., e.g. 10, 160, 170, 340, 435 MHz, 510, 680, 840, 850 MHz
6.8.	5...1019.99					—	—	—	—	—					●—		FAM	< 150Hz/rms (typ.<100Hz/rms)		FAM setting: FM, RMS, filter 10Hz/3kHz, select frequencies e.g. seq. 6.7.
7.																				Modulation modes
7.1.	470.0			-7 ⊗											●—	TP23*/U3	PMTR Vdc	-7dBm±2dB *4 4.7V	R639/U3	AM ext., *4 use for reference seq. 7.2. add. information
7.2.							x	x							●—	TP23*/U3	PMTR	ref*4 -6dBm±1dB	R633/U3	AM ext.; Vdc = 2,35V at TP23*/U3
7.3.							x	x				x			●—		FAM	m=50%±2%	R681/U3	AM mod. depth; signal to MOD IN: 2/20kHz, 20Hz∼, 0.5Vpp
7.4.							x	x				x			●—		FAM	m=80%±10%		20kHz∼, 0.9Vpp
7.5.	0.1...1019.99						x	x				x			●—		FAM	m=50%± 5%		2kHz∼, 0.5Vpp
7.6.	470.					x		x							●—		FAM	m=30%± 3%	R672/U3	AM int., mod. depth
7.7.	0.1...1019.99					x		x							●—		FAM	m=30%± 5%		
7.8.																	FAM			FM ext., FAM setting: FM, P+P/2, filter, 10Hz/200 kHz
7.9.	100.0			-7 ⊗			x		x			x			●—		FAM	Δf=38.5kHz±2kHz	R677/U3	FM ext., signal to MOD IN: 2kHz∼, 0.5Vpp
7.10.							x		x			x			●—		FAM	Δf=38.5kHz±2kHz		20Hz/20kHz∼, 0.5Vpp
7.11.							x		x			x			●—		FAM/ Dist.mtr.	Δf=75kHz± 1kHz K <1%		1kHz∼, 1Vpp
7.12.						x			x						●—		FAM	Δf=26kHz±0.3kHz	R675/U3	FM int.; FAM setting: FM, P+P/2, filter 10Hz/200 kHz
7.13.	0.1...170.0					x			x						●—		FAM	Δf=26kHz± 1kHz		
8.																				Video
8.1.									x	x		—	—			TP23*/U3	C/T	5.5MHz±10kHz sound c.±0.2%	C556/U3 C552/560/564	sound carrier sound car. 4.5/6.0/6.5MHz (selected by solder links)
8.2.	470.0			-7 ⊗				—	—	x			CVBS white		●—		SPA	-16dB± 1dB	R645/631/U3	residual RF carrier; SPA setting: BW=300 kHz, SW = 5MHz ST 5ms, Zero
																TP23*/U3	OSC	0.8±0.2V/ 4.7V		add. information, (CVBS = 1 Vpp)
8.3.	30...1019.99									x					●—		SPA	-16dB±2dB		residual RF carrier; select some frequencies
8.4.	470.0									x			Multib.		●—		SPA	* <-3dB	C574/U3	video bandwidth, apply to VIDEO IN: Multiburst 0.8-8MHz * use for reference 0.8 MHz
8.5.							x		x	x			CVBS red		●—		SPA	-13dB +0/-2dB	R696/U3	sound carrier FM
8.6.								—	—	x					●—		SPA	≥ 50dB	R643/U3	non harmonics (apply CVBS 1Vpp) level ratio RF carrier to fc±1.1MHz if neces. check video bandwidth, see seq. 8.4. and alter value R643/U3

Seq.	Keyboard operation FREQ MHz	FREQ MHz	SWEEP TIME (s)	LEVEL dBm	mV/µV/V	MODULATION INT	EXT	AM	FM	VIDEO	SWEEP SINGLE	CONT	REMOTE contr.	inputs MOD IN	VIDEO IN	measured via: outputs SWEEP T. OUT	RF OUT	test point	measuring instrument (see 7.2.)	measured value	adjustment control position	remarks general: for the correct sequence of pushbutton actions see operating manual
8.7.	470.0			-7 ⊗			x		x	x				x	—		●—		FAM	40kHz±2kHz	R692/U3	dev. sound carrier; signal to MOD IN: 5kHz ~, 0.5Vpp FAM: FM, P+P/2, filter 10Hz/200kHz, freq.475.5MHz
8.8.						x			x	x				—	—		●—		FAM	40kHz±2kHz		dev. sound carrier int; if neces. repeat seq.8.6.
8.9.							x	x		x				x			●—		FAM	m=30%±2%	R704/U3	AM sound carrier; signal to MOD IN: 5kHz ~ 0.5Vpp FAM: AM, P+P/2, filter 10Hz/2kHz, freq.475.5MHz
8.10.						x		x		x				—	—		●—		FAM	m=30%±2%		AM sound carrier int., if neces. repeat seq.8.8.
8.11.	196.250			-47 ⊗						x					CVBS		●—		CTV		control video settings by colour TV, CVBS = 1 Vpp into 75 Ω (pos. polarity)	
9.1.	65.0	50.0	.05	-7 ⊗								x				○—			C/T	250ms		Frequency sweep; sweep period = sweep time + fly-backt. (fly-backtime = 200 ms)
9.2.			1.0									x				○—			C/T	1200ms		
9.3.			20.									x				○—			C/T	20200ms		
9.4.											x						●—		C/T	65... 115 MHz		 50 x 1 MHz steps from 65 MHz up to 115 MHz
9.5.	65/540,	5.0	.05									x					●—		SPA	Δf=5MHz		SPA setting: BW=100kHz,
9.6.	720/920	5.0	.05									x					●—		SPA	Δf=5MHz		SW=1MHz, ST=1 s
9.7.	65.0	0.05	.05									x					●—		SPA	Δf=50kHz±5kHz		SPA setting: BW=10kHz, SW=1kHz, ST=1 s
9.8.	65.0	50.0	.05									x				○—			OSC	0.5Vpp±15mVpp	R626/U2	sweep ramp Vdc = 0V±2mV during fly-back
10.													x									<u>IEEE/IEC-bus</u> (select device address) check major front panel controls via a suitable computer or IEEE/IEC-bus controller (see operating manual chapter 3.4.10).

RF units PM 5390

The following table 7.3.2. should be used during the repair procedure of the RF units 1 and 2 and gives more detailed information in this part. For final checks of the complete instrument the previous table 7.3.1., seq. 1.0 ... 10 must be used, especially seq. 4.1... 5.8. output level.

RF units 1 and 2 are mounted to the connection board RF (813). All screening covers of the RF units must be closed and the specified warming-up time must be finished.

7.3.2 Table of checks and adjustments RF units

Seq.	Keyboard operation FREQ MHz	FREQ MHz	SWEEP TIME (s)	LEVEL dBm	MODULATION INT	EXT	AM	FM	VIDEO	±STEP freq.	level	measured via: inputs MOD IN	VIDEO IN	outputs SWEEP T. OUT	RF OUT	test point	measuring instrument (see 7.2.)	measured value	adjustment, control position	remarks
																				general: for the correct sequence of pushbutton actions see operating manual
1.																				frequency subranges, C/T setting: gate time 1 s except seq.1.2.
1.1.	1000.00			-7 dBm											●		C/T	1000MHz±100Hz	RF-U2/C563	time base, adjustment after 80 minutes
1.2.	0.100			-7 dBm											●		C/T	100kHz±1Hz		subrange 1, initial freq. (VCO1a/VCO3), C/T setting: gate t.10 s
1.3.	80/169														●		C/T	80/169MHz±1×10^{-6}		subrange 1 (VCO 1a/VCO 3)
1.4.	170/240														●		C/T	170/240MHz±1×10^{-6}		subrange 2 (VCO 1c/VCO 3)
1.5.	339.999														●		C/T	339.999MHz±1×10^{-6}		subrange 2, final frequency (VCO 1c/VCO 3)
1.6.	339.999 339.999															RF-U1 RF-U1	Vdc C/T	4 V ±0.5 V 39.0625 kHz	RF-U1/L816	VC03, measured at collector 363 VC03, measured at IC 308 pin 3 — adjust by more/less compression of coil 816
1.7.	340/410														●		C/T	340/410MHz±1×10^{-6}		subrange 3 (VCO 1a)
1.8.	509.999														●		C/T	509.999MHz±1×10^{-6}		end subrange 3 (VCO 1a)
1.9.	510/590														●		C/T	510/590MHz±1×10^{-6}		subrange 4 (VCO 1b)
1.10.	679.999														●		C/T	679.999MHz±1×10^{-6}		end subrange 4, final frequency (VCO 1b)
1.11.	680/760														●		C/T	680/760MHz±1×10^{-6}		subrange 5 (VCO 1c)
1.12.	849.999														●		C/T	849.999MHz±1×10^{-6}		subrange 5, final frequency (VCO 1c)
1.13.	850/930														●		C/T	850/930MHz±1×10^{-6}		subrange 6 (VCO 1d)
1.14.	1019.99														●		C/T	1019.99MHz±1×10^{-6}		subrange 6, final frequency (VCO 1d)
2.																				RF level, adjustments after 30 minutes
2.1.	470.			-7 dBm												RF-U1	SV (50)	-1dBm±1dB	RF-U1/R638	measured at mixer 851 pin 4
2.2.	470.															RF-U1	Vdc	4.5V±0.2V		measured at OP301 pin 6
2.3.	340...1019.99	20.0								x					●		PMTR	-7dBm±2dB	RF-U1/R697	if neces. move position R697 or ground point at freq. 340 MHz
2.4.	1019.99														●		PMTR	-7dBm±2dB	RF-U1/C547	value may be altered 1.5 pF...4.7 pF
2.5.	0.1...20.0	1.0								x					●		PMTR	-7dBm±2dB	RF-U1/R721	lower freq. range, (add. RF-U1/R724 may be altered)
2.6.	20...340	20.0								x					●		PMTR	-7dBm±2dB	RF-U1/C595	adjust only in freq. range 280 MHz...320 MHz
2.7.	0.1...1019.99														●		PMTR	-7dBm±dB	RF-U1/R638	complete freq. range, adjustment < 0.5 dB
3.0.																				RF level, pin diode attenuator
3.1.	470.0			-7 dBm											●		PMTR	-7dBm*2		*2 use for ref. value seq. 3.2...3.4., set PMTR to dB [REF]
																LP1/U2	Vdc	+ 3.4V±50mV	R681/U2 }*3	add. info. only, test pt. LP1/U2 or RF-U1/VR2
3.2.				-7... -16							x				●		PMTR	ref*2 0...-9±0.3dBm	R681/U2 }*3	single 1 dBm steps
3.3.				-107...-116							x				●		PMTR	ref*2 0...-9±0.3dBm		remove plug S2/unit 2 (coarse attenuator ≙ 100dBm not active)
3.4.				-117...-127							x				●	LP1/U2	PMTR	ref*2 -10...-20±2dBm		add. info. only, max. atten.-20dB at test pt. LP1/U2 Vdc ≈ 1.89V

*3 if tolerance exceeds close solder joint "E"/U1
repeat seq.3.2. to 3.4.(software I-A.1/II-A.1)

Seq.	Keyboard operation: FREQ MHz	ΔFREQ MHz	SWEEP TIME (s)	LEVEL dBm	MODULATION: INT	EXT	AM	FM	VIDEO	measured via: inputs: MOD IN	VIDEO IN	outputs: SWEEP T. OUT	RF OUT	test point	measuring instrument (see 7.2.)	measured value	adjustment, control position	remarks general: for the correct sequence of pushbutton actions see operating manual
4.																		spectral purity
4.1.	100.0			-7									●—		SPA	<-56 dB		non harmonics, check level ratio fref = 39.0625 kHz to RF carrier SPA setting: BW = 3 kHz, SW = 20 kHz, ST = 50 ms
4.2.	0.1...510			-7									●—		SPA	<-30 dBc		harmonics PM 5390 — level ratio 2nd/3rd harmonics to RF carrier freq. range 0.1-340 MHz all harmonics
4.3.				0									●—		SPA	<-30 dBc		harmonics PM 5390S — SPA setting: BW = 300 kHz, SW = 100 MHz, ST = 5ms
4.4.				+7									●—		SPA	<-25 dBc		
4.5.				+13									●—		SPA	<-20 dBc		
4.6.	0.1...339.999			-7									●—		SPA	<-30 dBc		non harmonics, select some frequencies (PM 5390/PM5390S)
4.7.	160.0			-7									●—		SPA	<-30 dBc	RF-U1/L808/809	check freq. 190 MHz, adjust by more/less compression of coils
4.8.	340...1019.99			-7									●—		SPA	<-40 dBc		
4.9.	100.			-7									●—		SPA	≤-67 dBc	RF-U1/C599	check at freq. 510 MHz, adjust to minimum
4.10.	340...679	20		-7									●—	RF-U2	SV	≥135mVrms... ≤300mVrms	RF-U2/R616	base signal level, oscillator VCO2a (ser. LO 04 onw.) measured at IC303 pin 16
4.11.	680...1019	20		-7									●—	RF-U2	SV	≥135mVrms... ≤150mVrms	RF-U2/R626	base signal level, oscillator VCO2b (ser. LO 04 onw.) measured at IC303 pin 16
4.12.	840/1000			-7									●—		FAM	< 250Hz/rms		residual FM; FAM setting: FM, RMS, filter 10Hz/3kHz
4.13.	5...1019.99			-7									●—		FAM	<100 Hz/rms		FAM setting: FM, RMS, filter 0.3/3kHz check some freq. , e.g. 10, 160, 170, 340, 435, 510, 680, 840, 850MHz
5.																		Modulation modes
5.1.	0.1...1019.99			-7		x	x			x			●—		FAM	m = 50%±5%	R681/U3	AM ext., signal to MOD IN: 10 kHz∼, 0.5 Vpp, check at freq.: 20, 150, 190, 320, 490, 530, 660, 850, 1000 MHz
5.2.	0.1...1019.99			-7		x	x			x			●—		FAM	m> 80%		AM ext., signal to MOD IN: 20 kHz∼, 1 Vpp; check some RF freq.
5.3.	100.0			-7		x		x		x			●—		FAM	Δf = 75±1kHz	RF-U1/C558	FM ext., signal to MOD IN: 20 kHz∼, 1 Vpp; adjust C588 ∥ 1.2pF...3.3pF
5.4.	100/300			-7	x			x					●—		FAM	Δf = 25±2kHz		FM intern
5.5.																		Video, SPA setting: BW = 300 kHz, SW = 5 MHz, ST = 5ms, Zero
5.6.	220/850			-7					X		CVBS		●—		SPA	-16dB±1dB	U3/R645/631	residual RF carrier, signal to VIDEO IN: CVBS white 1 Vpp

8. SAFETY INSPECTION AND TESTS AFTER REPAIR AND MAINTENANCE IN THE PRIMARY CIRCUIT

8.1. GENERAL DIRECTIVES

- Take care that creepage distances and clearances have not been reduced
- Before soldering, wires:
- should be bent through the holes of solder tags, or wrapped round the tag in the form of an open U, or, wiring ridigity shall be maintained by cable clamps or cable lacing.
- Replace all insulating guards and -plates.

8.2. SAFETY COMPONENTS

Components in the primary circuit may only be renewed by components selected by Philips, see also chapter 9.1.

8.3. CHECKING THE PROTECTIVE EARTH CONNECTION

The correct connection and condition is checked by visual control and by measuring the resistance between the protective-lead connection at the plug and the cabinet/frame. The resistance shall not be more than 0.5 Ω. During measurement the mains cable should be moved. Resistance variations indicate a defect.

8.4. CHECKING THE INSULATION RESISTANCE

Measure the insulation resistance at U = 500 Vdc between the mains connections and the protective lead connections. For this purpose set the mains switch to ON. The insulation resistance shall not be less than 2 MΩ.

Note:
2 MΩ is a minimum requirement at 40^{o} C and 95 % relative humidity. Under normal conditions the insulation resistance should be much higher (10 to 20 MΩ).

9. SPARE PARTS

9.1. GENERAL

Standard Parts

Electrical and mechanical parts replacement can be obtained through your local Philips organisation or representative. However, many of the standard electronic components can be obtained from other local suppliers. Before purchasing or ordering replacement parts, check the parts list for value, tolerance, rating and description.

NOTE: Physical size and shape of a component may affect instrument performance, particularly at high frequencies. Always use direct-replacement components, unless it is known that a substitute will not degrade instrument performance.

Special Parts

In addition to the standard electronic components, some special components are used;
- Components, manufactured or selected by Philips to meet specific performance requirements.
- Components which are important for the safety of the instrument marked with 'S' in the parts list.

ATTENTION: Both type of components may only be replaced by components obtained through your local Philips organisation.

9.2. STATIC SENSITIVE COMPONENTS

This instrument contains electrical components that are suspectible to damage from static discharge. Servicing static-sensitive assemblies or components should be performed only at a static-free work station by qualified service personnel.

9.3. HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

CAUTION: Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

9.4. SOLDERING TECHNIQUES

Working method:
- Carefully unsolder one after the other the soldering tags of the semi-conductor.
- Remove all superfluous soldering material. Use a sucking iron or sucking litze wire.
- Check that the tags of the replacement part are clean and pre-tinned on the soldering places.
- Locate the replacement semi-conductor exactly on its place, and solder each tag to the relevant printed conductor on the circuit board.

NOTE: Bear in mind that the maximum permissible soldering time is 10 seconds during which the temperature of the tags must not exceed 250 ^{o}C. The use of solder with a low melting point is therefore recommended.
Take care not to damage the plastic encapsulation of the semi-conductor (softening point of the plastic is 150 ^{o}C).

ATTENTION: When you are soldering inside the instrument it is essential to use a low-voltage soldering iron, the tip of which must be earthed to ground of the instrument.

Suitable soldering irons should have temperature control and different types of nozzles (pin point tips), e.g. Weller Magnastat WTCP or WECP, Ersa TC 70/24 V.

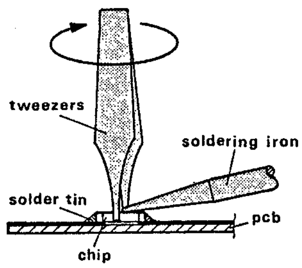
If a higher wattage-rating soldering iron is used on the etched circuit boards (especially on the RF-units), excessive heat can cause the etched circuit wiring to seperate from the board base material.
In general use short-time heating with high tip temperature at a small point, avoid long time heating.

Chip components

- Do not use unsoldered chips again
- For replacement take only specified components
- Do not use any adhesive to fix components
- Replaced chips must positioned flat on the pcb before soldering starts
- Use only resin-core solder tin with silver (60, 36, 4 Ag)

Working method:

- Carefully unsolder both soldering tags of the chip component. Avoid to lift printed conductor on the pcb.
- Remove all superfluous material. Use a sucking iron or sucking copper litze wire.
- Locate the replacement chip exactly in place
- An additional fixing point made by solder-tin could be efficient.
- Solder each tag to the relevant printed conductor on the pcb
- After a short cooling period resolder again the first soldered joint (tension release of the chip).



unsolder chip components

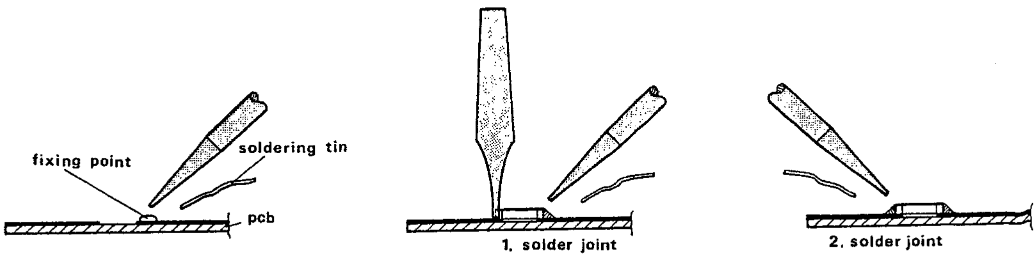


Fig. 14 Replacement of chip components

9.5. PARTS LIST PM 5390

9.5.1. MECHANICAL PARTS, miscellaneous, parts not on units

Item	Fig.	Quantity	Order number		Description
1	31	1	5322 447 90354		COVER
2	31	4	5322 462 10222		FOOT (BOTTOM SIDE)
3		2	5322 520 34164		BEARING BUSH
4		2	5322 530 84075		SPRING
5		2	5322 528 34101		RATCHET
6		2	5322 532 51481		RING FOR HANDLE
7		2	5322 498 54048		ARM FOR HANDLE
8		1	5322 498 54051		CARRYING HANDLE
9		2	5322 414 30043		KNOB
10		1	5322 321 20697	*S	MAINS CABLE
11	32	1	5322 256 34081	*S	FUSE HOLDER
12	32	4	5322 462 44176		FOOT (REAR SIDE)
751		1	5322 146 40342	*S	MAINS TRANSFORMER until LO04..
751			5322 146 50205	*S	MAINS TRANSFORMER from LO05...onw.
851	31	1	5322 276 14128	*S	MAINS SWITCH
13		1	5322 447 94363	*S	PROTECTION CAP P.851
856	31	1	4822 253 30014	*S	FUSE 315MAT
-		1	4822 253 30018	*S	FUSE 630MAT
857	32	1	5322 267 30416	*S	MAINS SOCKET/FILTER
840	32	1	5322 266 51002		IEEE BUS CONNECTOR
14	31	3	5322 267 10004		BNC CONNECTOR
814		1	5322 210 70083		RF ATTENUATOR UNIT
854		1	5322 267 10136		BNC CONNECTOR RF OUTP.
854A		1	5322 321 20811		RF OUTPUT CONNECT.PIECE PM5390 series LO 01...03
841	32	1	5322 277 24053		BATT.SWITCH (REAR S.)
842,843	32	2	5322 277 24045		DEV.ADDRESS SK 1-4
844	32	1	5322 277 24053		DEV.ADRESS SK 5
15		1	5322 321 20812		FLAT CABLE CON.U1/6
16		28	5322 276 11191		PUSHBUTTON (KEYB.)
17	31	28	5322 414 70031		CAP FOR PUSHBUTTON
18	31	1	5322 459 20276		WINDOW F.DISPLAY
19		1	5322 466 91448		RETAINING STRIP U1/3
20		17	5322 255 40336		IC SOCKET,14POLE
21		3	5322 255 44107		IC SOCKET,16POLE
22		1	5322 255 44055		IC SOCKET,20POLE
23		4	5322 255 44229		IC SOCKET,24POLE
24		2	5322 255 44234		IC SOCKET,28POLE
25		6	5322 255 44235		IC SOCKET,40POLE
501		1	4822 122 30128		CAPACITOR 4N7/100V
601		1	4822 116 51279	*S	RESISTOR 1MAO/MR30
760		1	5322 158 14034		COIL 220MUH
-		1	5322 390 24013		SILICON PASTE 142G
			5322 390 80129		SOLDERING TIN (60/36/4AG)

*S = safety component

9.5.2. ELECTRICAL PARTS

Some parts are lsited in chapter 9.5.1.

All metal film resistors not listed are of type MR 25±1% 0.4W (ordering code see end of this list).

*1 Please order loaded PROM directly via Philips Supply Center Hamburg (note software version).

ITEM	DESCRIPTION				ORDERING CODE
UNIT 1					
INTEGRATED CIRCUITS/U1					
301	INTEGR.CIRCUIT	MC3441P			5322 209 85464
302	INTEGR.CIRCUIT	HEF4518BP			5322 209 14064
303	INTEGR.CIRCUIT	HEF4077BP			4822 209 10223
304	INTEGR.CIRCUIT	MC3441P			5322 209 85464
305	INTEGR.CIRCUIT	HEF4738VP			5322 209 14509
306*1	INTEGR.CIRCUIT	HN462716,PROM (software version)			
307	INTEGR.CIRCUIT	N74LS02A			5322 209 85312
308,314	INTEGR.CIRCUIT	MC3441P			5322 209 85464
309,310	INTEGR.CIRCUIT	HEF40097BP			5322 209 14433
312	INTEGR.CIRCUIT	N74LS32A			5322 209 85311
313	INTEGR.CIRCUIT	CDP1823CE			5322 209 81779
311*1	INTEGR.CIRCUIT	HN462732G,PROM (software version)			
315	INTEGR.CIRCUIT	HEF4014BD			4822 209 10296
316	INTEGR.CIRCUIT	P8085AH			5322 209 50032
317	INTEGR.CIRCUIT	N74LS363N			5322 209 81776
318	INTEGR.CIRCUIT	P8155H			5322 209 14563
320	INTEGR.CIRCUIT	N74LS155N			4822 209 85752
321	INTEGR.CIRCUIT	ICL8212CPA			5322 209 81775
DIODES/U1					
401,402	DIODE	AAZ15			4822 130 30229
403	DIODE	BAW62			4822 130 30613
404	DIODE	AAZ15			4822 130 30229
CAPACITORS/U1					
501,505	CAP,SOLID ALU. SAL	22UF 20%	6.3V		4822 124 20989
502,509	CAPACITOR,CERAM	10NF 80%	100V		4822 122 30043
503,504	CAPACITOR,CERAM	22NF 80%	63V		5322 122 31795
506,508	CAPACITOR,CERAM	22NF 80%	63V		5322 122 31795
507	CAPACTTOR,CERAM	10PF 2%	100V		4822 122 31054
510	CAP,SOLID ALU. SAL	22UF 20%	6.3V		4822 124 20989
511	CAPACITOR,CERAM	22NF 80%	63V		5322 122 31795
512	CAPACITOR,CERAM	56PF 2%	63V		4822 122 31524
RESISTORS/U1					
603,615	RESISTOR-NETW.	8x4K7 5%	0,125W		5322 116 90132
604,613	RESISTOR-NETW.	4x4K7 5%	0,125W		5322 116 90131
CRYSTAL/U1					
801	CRYSTAL	6.000 MHz		HC18U	4822 242 70392
BATTERY/U1					
805	BATTERY	NICD-BATT.	3,6V		5322 138 10047

ITEM	DESCRIPTION		ORDERING CODE	
UNIT 2				
TRANSISTORS/U2				
330-333	TRANSISTOR	BC557B	4822 130 44568	
335	TRANSISTOR	BC338	4822 130 44121	*
336	TRANSISTOR	BC548B	4822 130 40937	
337,338	TRANSISTOR	BC338	4822 130 44121	
DIODES/U2				
401	DIODE,REFERENCE	BZV46-C2VO	4822 130 31248	
402,403	DIODE	AA144	5322 130 32161	
405	DIODE	BAW62	4822 130 30613	*
406,407	DIODE	AA144	5322 130 32161	
408,409	DIODE	BAW62	4822 130 30613	
INTEGRATED CIRCUITS/U2				
301	INTEGR.CIRCUIT	HEF4751VP	5322 209 10525	
302	INTEGR.CIRCUIT	N74LS09N	5322 209 85801	
303	INTEGR.CIRCUIT	MC1458N	4822 209 81349	
304,308	INTEGR.CIRCUIT	UA741N	5322 209 85957	
305,309	INTEGR.CIRCUIT	P8255A	5322 209 86126	
306	INTEGR.CIRCUIT	N74LS09N	5322 209 85801	
307	INTEGR.CIRCUIT	SN74HC4024	5322 209 82801	
310,314	INTEGR.CIRCUIT	HEF4066BP	5322 209 14104	
311	INTEGR.CIRCUIT	HEF4023BD	4822 209 10252	
312	INTEGR.CIRCUIT	HEF4520BP	5322 209 14189	
313	INTEGR.CIRCUIT	SN74LS05N	5322 209 84994	
315	INTEGR.CIRCUIT	SN7409N	5322 209 84464	
316	INTEGR.CIRCUIT	SN7406J-00	5322 209 86327	
CAPACITORS/U2				
501,503	CAPACITOR,CERAM	22PF 2% 100V	4822 122 31063	
502	CAPACITOR,CERAM	22NF 80% 63V	5322 122 31795	
504,506	CAP,ELEC.SAL	10UF 20% 16V	5322 124 14066	
508	CAPACITOR,CERAM	22PF 2% 100V	4822 122 31063	
509	CAP,ELEC.SAL	10UF 20% 16V	5322 124 14066	
510-512	CAPACITOR,CERAM	4,7NF 10% 100V	4822 122 30128	
515-517	CAPACITOR,CERAM	22NF 80% 63V	5322 122 31795	
518	CAPACITOR,CERAM	4,7NF 10% 100V	4822 122 30128	
520-525	CAPACITOR,CERAM	22NF 80% 63V	5322 122 31795	
RESISTORS/U2				
601	RESISTOR-NETW.	8x15K 5% 0,125W	5322 116 60192	
626	POTM.TRIMMING	4K7 LIN 0,1W	4822 100 10236	
628	RESISTOR-NETW.	8x4K7 5% 0,125W	5322 116 90132	
651	RESISTOR-NETW.	4x47K 5% 0,125W	5322 116 60189	
681	POTM.TRIMMING	2K2 LIN 0,1W	4822 100 10027	
607	RESISTOR	453K 1% 0,3W	5322 116 52443	

* only PM 5390 S

ITEM	DESCRIPTION				ORDERING CODE
UNIT 3					
TRANSISTORS/U3					
301,308	TRANSISTOR	BC548B			4822 130 40937
302	TRANSISTOR	BC557			4822 130 44256
303	TRANSISTOR	BC338			4822 130 44121
304	INTEGR.CIRCUIT	SG3823N			5322 209 84862
305	TRANSISTOR	BC558B			4822 130 44197
306	TRANSISTOR	BC548C			4822 130 44196
307	INTEGR.CIRCUIT	MC3386P (CA3086)			5322 209 86236
309	TRANSISTOR	BF240			4822 130 40902
310	TRANSISTOR	BC548B			4822 130 40937
311	TRANSISTOR	BF450			4822 130 44237
DIODES/U3					
401	DIODE,REFERENCE	BZV46-C2V0			4822 130 31248
402,403	DIODE	BAW62			4822 130 30613
410	DIODE	BB909A			5322 130 32162
INTEGRATED CIRCUITS/U3					
351,352	INTEGR.CIRCUIT	SN74LS05N			5322 209 84994
353-356	INTEGR.CIRCUIT	HEF4066BP			5322 209 14104
357	INTEGR.CIRCUIT	UA741N			5322 209 85957
CAPACITORS/U3					
501,505	CAPACITOR,CERAM	10NF	80%	100V	4822 122 30043
502	CAP,ELEC.SAL	33UF	20%	6,3V	4822 124 40963
504,506	CAP,ELEC.SAL	10UF	20%	16V	5322 124 14066
507,517	CAPACITOR,CERAM	10NF	80%	100V	4822 122 30043
508	CAP,ELEC.SAL	10UF	20%	16V	5322 124 14066
511,512	CAP,ELEC.SAL	22UF	20%	10V	4822 124 20943
513	CAPACITOR,FOIL	220NF		63V	5322 121 44258
514	CAP,ELECTROLYT.	150UF	50%	6,3V	4822 124 20672
515	CAPACITOR,CERAM	33PF	2%	100V	5322 122 31995
516	CAPACITOR,CERAM	*6P8	2%	100V	5322 122 31994
518,521	CAP,ELEC.SAL	10UF	20%	16V	5322 124 14066
519	CAP,ELEC.SAL	22UF	20%	6,3V	4822 124 20989
522	CAPACITOR,CERAM	10NF	80%	100V	4822 122 30043
523	CAP,ELECTROLYT.	220UF	50%	16V	4822 124 20693
531	CAP,ELEC.SAL	2,2UF	20%	16V	4822 124 40902
532	CAP,ELEC.SAL	47UF	20%	6,3V	4822 124 40901
533-535	CAPACITOR,FOIL	100NF	10%	50V	5322 122 30108
541	CAP,ELECTROLYT.	47UF	20%	10V	5322 124 21391
542,550	CAPAITOR,CERAM	220PF	10%	100V	4822 122 30094
543,549	CAP,ELECTROLYT.	10UF	50%	16V	5322 124 14066
544	CAPACITOR,CERAM	150NF	10%	50V	4822 121 40231
545	CAPACITOR,FOIL	100NF	10%	50V	5322 122 30108
546	CAP.ELECTROLYT	2.2UF	20%	16V	4822 124 10204
547	CAP.ELECTROLYT	220UF	20%	10V	4822 124 40181
548	CAPACITOR,FOIL	1MU	10%	50V	5322 121 41883
552,556	CAPACITOR,TRIMM	1-6PF		400V	5322 125 54006
553,554	CAPACITOR,CERAM	56PF	2%	100V	4822 122 31524
557,558	CAPACITOR,CERAM	18PF	2%	100V	5322 122 31061
560	CAPACITOR,TRIMM	1 - 6PF		400V	5322 125 54006
561	CAPACITOR,CERAM	15PF	2%	100V	4822 122 31058
562	CAPACITOR,CERAM	22PF	2%	100V	4822 122 31063
563	CAPACITOR,CERAM	39PF	2%	100V	5322 122 31996
564	CAPACITOR,TRIMM	2,5-25PF		250V	5322 125 54058
565,568	CAPACITOR,CERAM	22NF	80%	63V	5322 122 31795
566	CAPACITOR,CERAM	68PF	2%	100V	5322 122 31997
567	CAPACITOR,CERAM	1NF	10%	100V	4822 122 30027
569,571	CAPACITOR,CERAM	22NF	80%	63V	5322 122 31795
570	CAPACITOR,CERAM	47PF	2%	100V	4822 122 31072
572	CAP,ELECTROLYT.	47UF	20%	10V	5322 124 21391
573	CAPACITOR,CERAM	100NF	10%	50V	5322 122 32002
574	CAPACITOR,CERAM	* 33PF	2%	100V	5322 122 31995

* value may be altered in test.

ITEM	DESCRIPTION				ORDERING CODE
RESISTORS/U3					
609,610	RESISTOR-NETW.	8x4K7	5%	0,125W	5322 116 60191
631,639	POTM.TRIMMING	2K2	LIN	0,1W	4822 100 10027
645,677	POTM.TRIMMING	2K2	LIN	0,1W	4822 100 10027
671,674	RESISTOR,HT	10M			4822 110 72214
681	POTM,TRIMMING	470E	LIN	0,1W	4822 100 10023
692,696	POTM,TRIMMING	22K	LIN	0,1W	5322 101 44041
COILS/U3					
801	COIL	6UH			5322 157 54136
802	COIL	100 UH			5322 158 10243
UNIT 4					
TRANSISTORS/U4					
351,352	TRANSISTOR	BC338			4822 130 44121
353,354	TRANSISTOR	BC558B			4822 130 44197
355,356	TRANSISTOR	BC636			4822 130 44283
357-360	TRANSISTOR	BC558B			4822 130 44197
361,362	TRANSISTOR	BC338			4822 130 44121
363,364	TRANSISTOR	BC636			4822 130 44283
365-368	TRANSISTOR	BC558B			4822 130 44197
369,370	TRANSISTOR	BC338			4822 130 44121
371,372	TRANSISTOR	BC558B			4822 130 44197
373-375	TRANSITOR	BC636			4822 130 44283
376	TRANSITOR	BC548B			4822 130 40937
377	TRANSISTOR	BC338			4822 130 44121
378,379	TRANSISTOR	BC558B			4822 130 44197
380,381	TRANSISTOR	BC636			4822 130 44283
382,383	TRANSISTOR	BC558B			4822 130 44197
384-389	TRANSISTOR	BC636			4822 130 44283
INTEGRATED CIRCUITS/U4					
301	INTEGR.CIRCUIT	N74LS154N			5322 209 86085
302	INTEGR.CIRCUIT	P8279			5322 209 86243
303	INTEGR.CIRCUIT	SN74LS03N			5322 209 85265
304	INTEGR.CIRCUIT	N74LS155N			5322 209 85752
305	INTEGR.CIRCUIT	SN74LS05N			5322 209 84994
306	INTEGR.CIRCUIT	N74LS00N			5322 209 84823
307	INTEGR.CIRCUIT	NE555N			4822 209 80775
308	INTEGR.CIRCUIT	SN74LS248N			5322 209 85789
CAPACITORS/U4					
501-505	CAPACITOR,CERAM	22NF	80%	63V	5322 122 31795
506	CAP,ELECTROLYT.	68UF	50%	6,3V	4822 124 20671
507	CAP,ELEC.TANTAL	3,3UF	20%	16V	5322 124 14069
508	CAPACITOR,CERAM	22NF	80%	63V	5322 122 31795
RESISTORS/U4					
601,602	RESISTOR-NETW.	8x4K7	5%	0,125W	5322 116 90132
603	RESISTOR-NETW.	8x2K2	5%	0,125W	5322 116 60193
UNIT 5					
DIODES/U5					
416-426	LED	CQY54			4822 130 30914
DISPLAY/U5					
401-412	DISPLAY	HP5082-7730			5322 130 34389
413	DISPLAY	HP5082-7732			5322 130 34985
414,415	DISPLAY	HP5082-7730			5322 130 34389

ITEM	DESCRIPTION				ORDERING CODE

UNIT 7

TRANSISTORS/INTEGRATED CIRCUITS/DIODES

301	TRANSISTOR	BD139			4822 130 40823
302	INTEGR.CIRCUIT	UA723CN			5322 209 85889
401	RECTIFIER	SKB2/08L5			5322 130 32031
403	DIODE,REF.	BZX79-C39			4822 130 34145

CAPACITORS

501	CAP.ELECTROLYT.	220UF		63V	4822 124 20801
502,503	CAP.ELECTROLYT.	4,7UF		63V	4822 124 20726
505	CAP.CERAMIC	470PF	10%	100V	5322 122 31796
506	CAP.ELECTROLYT.	100UF		63V	5322 124 21271
507	CAP.CERAMIC	100NF	10%	50V	5322 122 32002

UNIT 10

TRANSISTORS/U10

301	TRANSISTOR	BD139			4822 130 40823

DIODES/U10

401,402	RECTIFIER	BY260-200			4822 130 32145
403,404	DIODE	BY206			4822 130 30839
405	DIODE,REFERENCE	BZX79-B36			4822 130 34368
410	RECTIFIER	SKB2/08L5A			5322 130 32031 *2

INTEGRATED CIRCUITS/U10

351	INTEGR.CIRCUIT	78GU1C			5322 209 85565
352	INTEGR.CIRCUIT	UA7812UC			5322 209 86176
353	INTEGR.CIRCUIT	UA7912CU			5322 209 81179
354,355	INTEGR.CIRCUIT	LM340T-5.0			4822 130 41223
356	INTEGR.CIRCUIT	SN74LS05N			5322 209 84994
360	INTEGR.CIRCUIT	UA7824UC			5322 209 86026

CAPACITORS/U10

503	CAP,ELECTROLYT	47UF	50%	63V	4822 124 20733
504	CAP,ELECTROLYT.	220UF	50%	63V	4822 124 20801
505	CAP,ELECTROLYT.	10UF	50%	63V	5322 124 21356
506	CAP,ELECTROLYT.	4,7UF	50%	63V	4822 124 20726
507,511	CAP,ELEC.SAL	1,5UF	20%	25V	4822 124 20942
508,512	CAP,ELECTROLYT.	22UF	50%	25V	4822 124 20698
509,513	CAPACITOR,CERAM	10NF	50%	100V	4822 122 31414
510	CAP,ELECTROLYT.	6800UF	30%	25V	5322 124 40781
514	CAP,ELECTROLYT.	2200UF	30%	40V	4822 124 40351
515,517	CAP,ELEC.SAL	1,5UF	20%	25V	4822 124 20942
516,518	CAP,ELECTROLYT.	22UF	50%	25V	4822 124 20698
519	CAPACITOR,CERAM	10NF	20%	100V	4822 122 31414
520	CAP,ELECTROLYT.	10000UF	30%	19V	5322 124 44055
521	CAP,ELECT.SAL	1,5UF	20%	25V	4822 124 20942
522	CAP,ELECTROLYT.	22UF	50%	25V	4822 124 20698
523	CAPACITOR,CERAM	22NF	80%	63V	5322 122 31795
524,527	CAPACITOR,CERAM	4,7NF	10%	100V	4822 122 30128
525,526	CAPACITOR,CERAM	22NF	80%	63V	5322 122 31795
528,529	CAPACITOR,CERAM	22NF	80%	63V	5322 122 31795
530	CAP,ELECT.SAL	22UF	20%	10V	4822 124 20943
540	CAPACITOR,CERAM	22NF	80%	63V	5322 122 31795 *2
541	CAP,ELECTROLYT.	10000UF	30%	63V	5322 124 44045 *2
542	CAP,ELEC.SAL	1UF	20%	40V	4822 124 40903 *2
543	CAP,ELECTROLYT.	10UF	50%	40V	4822 124 20708 *2

*2 only PM 5390 S

ITEM	DESCRIPTION				ORDERING CODE
RESISTORS/U10					
601	RESISTOR,M.FILM	2E26	1%	0,4W	5322 116 51835
609	POTM,TRIMMING	1K	LIN	0,1W	4822 100 10037
611,612	RESISTOR,M.FILM	2E26	1%	0,4W	5322 116 51835
622	RESISTOR,M.FILM	2E26	1%	0,4W	5322 116 51835 *2
RELAIS/U10					
801-806	RELAY,REED				4822 280 20064
807-808	RELAY,REED				5322 280 80511
810	RELAY,REED				5322 280 80511 *2
RF UNIT 1					*2 ONLY PM 5390S
TRANSISTORS/RF-U1					
351	TRANSISTOR	BF480			5322 130 44582
352	TRANSISTOR	BFR96/02			5322 130 44911
353,354	TRANSISTOR	BFR96/02			5322 130 44911
355	TRANSISTOR	BC548B			4822 130 40937
358-362	TRANSISTOR	BC548A			4822 130 40948
363	TRANSISTOR	BD677			4822 130 41484
364	TRANSISTOR	BF480			5322 130 44582
365	TRANSISTOR	BC548B			4822 130 40937
366	TRANSISTOR	BFR96/02			5322 130 44911
DIODES/RF-U1					
401,402	DIODE	BAW62			4822 130 30613
403	DIODE	BB909A			5322 130 32162
405	DIODE	BB909A			5322 130 32162
406-408	DIODE	BB405B			5322 130 34953
409,410	DIODE	HP5082-2811			5322 130 34018
411-419	DIODE	BA379			5322 130 80399
420	DIODE,REFERENCE	BZX79-B5V6			4822 130 34173
421-423	DIODE	BA379			5322 130 80399
424	DIODE	BA482			5322 130 34955
425,426	DIODE	BA379			5322 130 80399
427	DIODE	BAW62A			4822 130 30613
428	DIODE	BA379			5322 130 80399
431-435	DIODE	BAW62			4822 130 30613
437	DIODE	BB405B			5322 130 34953
438	DIODE	BAT85 (2 diodes)			4822 130 31983 LO 05 onw.
441	DIODE	BA379			5322 130 80399
INTEGRATED CIRCUITS/RF-U1					
301,302	INTEGR.CIRCUIT	UA741N			5322 209 85957
304	INTEGR.CIRCUIT	OM350			5322 209 81008
303,305	INTEGR.CIRCUIT	OM360			5322 209 81361
306	INTEGR.CIRCUIT	MWA320			5322 209 81778
307	INTEGR.CIRCUIT	UA7805CU			5322 209 84841
308	INTEGR.CIRCUIT	MC4044L			5322 209 85821
309	INTEGR.CIRCUIT	HEF4040BP			5322 209 14269
310,311	INTEGR.CIRCUIT	OM350			5322 209 81008
312	INTEGR.CIRCUIT	CA3179G			5322 209 81777
313	INTEGR.CIRCUIT	MWA130			5322 209 81783
314	INTEGR.CIRCUIT	REF-01CP			5322 209 82768 LO 05 onw.
CAPACITORS/RF-U1					
451-455	CAP,FEEDTROUGH	2,2NF	80%	160V	5322 122 70114
456	CAP,FEEDTROUGH	47PF	10%	160V	5322 122 70112
457-459	CAP,FEEDTROUGH	2,2NF	80%	160V	5322 122 70114
460	CAP,FEEDTROUGH	47PF	10%	160V	5322 122 70113
461,462	CAP,FEEDTROUGH	2,2NF	80%	160V	5322 122 70114
464	CAPACITOR,CERAM	1P5	0,25PF	100V	5322 122 32101

ITEM	DESCRIPTION				ORDERING CODE
465	CAPACITOR,CERAM	15UF	10%	16V	4822 124 20977
466	CAPACITOR,CERAM	18PF	2%	100V	4822 122 31061
467*	CAPACITOR,CERAM	2,2PF	0,25PF	63V	5322 122 40399
468	CAPACITOR,CERAM	3P9	2%	63V	5322 122 34107
469	CAPACITOR,CHIP	820PF	80%	400V	5322 122 32001
470,480	CAPACITOR,CERAM	1NF	10%	63V	5322 122 40419
471,476	CAPACITOR,CERAM	4,7NF	10%	100V	4822 122 30128
472*	CAPACITOR,CERAM	1P0	0,25PF	63V	4822 122 30104
473,478*	CAPACITOR,CERAM	0P68	0,25PF	63V	5322 122 40411
475	CAP,ELECTROLYT.	15UF	10%	16V	4822 124 20977
481	CAPACITOR, CERAM	4,7NF	10%	100V	4822 122 30128
485	CAPACITOR, CERAM	0,68PF	0,25PF	63V	5322 122 40411
486	CAP.ELECTROLYT.	15UF	10%	16V	4822 124 20977
487	CAPACITOR, CERAM	15PF	10%	400V	5322 122 40417
488,489	CAPACITOR, CERAM	4,7NF	10%	100V	4822 122 30128
498,499	CAPACITOR, CERAM	4,7NF	10%	100V	4822 122 30128
490	CAPACITOR, CERAM	1NF	10%	63V	5322 122 40419
491	CAPACITOR, CERAM	1NF	10%	63V	5322 122 40418
494,495	CAPACITOR, CERAM	0,68PF	0,25PF	63V	5322 122 40411
496	CAPACITOR, CERAM	15UF	10%	16V	5322 124 20977
497	CAPACITOR, CERAM	8,2PF	0,25PF	400V	5322 122 40416
501,506	CAPACITOR,CHIP	1NF	10%	63V	5322 122 31998
502	CAPACITOR, CERAM	100N	10%	50V	5322 122 32002
503	CAPACITOR, CERAM	100PF	2%	63V	5322 122 40405
504	CAPACITOR, CERAM	220PF	2%	63V	5322 122 40407
505	CAPACITOR, CERAM	6,8PF	2%	100V	5322 122 31994
507	CAPACITOR, CERAM	1NF	10%	63V	5322 122 40419
508,514	CAPACITOR,CHIP	1NF	10%	63V	5322 122 31998
509	CAPACITOR,CHIP	820PF	80%	400V	5322 122 32001
510,511	CAPACITOR,CERAM	22NF	80%	63V	5322 122 31795
512,513	CAPACITOR,CHIP	820PF	80%	400V	5322 122 32001
515	CAPACITOR,CERAM	1NF	10%	63V	5322 122 40419
516,517	CAPACITOR,CHIP	1NF	10%	63V	5322 122 31998
518	CAPACITOR,CERAM	56PF	2%	63V	5322 122 40408
519	CAPACITOR,CHIP	1NF	10%	63V	5322 122 31998
520,524	CAPACITOR,CERAM	1NF	10%	63V	5322 122 40418
521,523	CAPACITOR,CERAM	6,8PF	0,25PF	63V	5322 122 40403
522	CAPACITOR,CERAM	10PF	2%	63V	5322 122 40397
525,527	CAPACITOR,CERAM	4,7PF	0,25PF	63V	5322 122 40423
526	CAPACITOR,CERAM	8,2PF	0,25PF	63V	5322 122 40413
528	CAPACITOR,CERAM	1NF	10%	63V	5322 122 40418
529,533	CAPACITOR,CHIP	1NF	10%	63V	5322 122 31998
530	CAPACITOR,CERAM	4,7NF	10%	100V	4822 122 30128
531	CAPACITOR,CERAM	1NF	10%	63V	5322 122 40419
532	CAPACITOR,CHIP	820PF	80%	400V	5322 122 32001
534	CAPACITOR,CERAM	22NF	80%	63V	5322 122 31795
535,536	CAPACITOR,CHIP	820PF	80%	400V	5322 122 32001
537,539	CAPACITOR,CHIP	1NF	10%	63V	5322 122 31998
538	CAPACITOR,CERAM	4,7NF	10%	100V	4822 122 30128
540,542	CAPACITOR,CHIP	1NF	10%	63V	5322 122 31998
541	CAPACITOR,CHIP	820PF	80%	400V	5322 122 32001
544	CAPACITOR,CERAM	OP68	0,25PF	63V	5322 122 40411
545,550	CAPACITOR,CHIP	220NF	10%	63V	5322 122 31999
543,548	CAPACITOR,CHIP	1NF	10%	63V	5322 122 31998
546	CAPACITOR,CERAM	0,68PF	0,25PF	500V	4822 122 31213
547	CAPACITOR, CERAM	2,2NF	0,25PF	63V	5322 122 40399
551	CAP.ELEC.SAL	15UF	20%	16V	4822 124 20977
552,556	CAPACITORS,CERAM	22NF	80%	63V	5322 122 31795
553	CAPACITORS,ELECT.	2,2UF	20%	25V	4822 124 21255
554,555	CAPACITORS,ELECT.SAL	15UF	20%	16V	4822 124 20977

* may be altered in test

ITEM	DESCRIPTION				ORDERING CODE
557	CAPACITOR,ELECT.SAL	15UF	20%	16V	4822 124 20977
559	CAPACITOR,CERAM	1,2PF	0,25PF	63V	5322 122 40415
560	CAP,ELEC.SAL	22UF	20%	6.3V	4822 124 20989
561	CAP,ELEC.SAL	4.7UF	20%	25V	4822 124 10367
562,563	CAP.ELEC.SAL	15UF	20%	16V	4822 124 20977
564	CAPACITOR,CHIP	220NF	10%	63V	5322 122 31999
565	CAPACITOR,CERAM	100N	10%	50V	5322 122 32002
566	CAPACITOR,CHIP	820PF	80%	400V	5322 122 32001
567	CAPACITOR,CERAM	22NF	80%	63V	5322 122 31795
568	CAPACITOR,CERAM	4,7PF	0,25PF	63V	5322 122 40412
569	CAP,ELEC.SAL	15UF	20%	16V	4822 124 20977
570	CAPACITOR,CERAM	2,7PF	0,25PF	63V	5322 122 40448
571	CAPACITOR,CERAM	100N	10%	50V	5322 122 32002
572,574	CAPACITOR,CERAM	1NF	10%	63V	5322 122 40419
573,575	CAPACITOR,CERAM	5,6PF	0,25PF	63V	5322 122 40402
576	CAPACITOR,CERAM	1NF	10%	63V	5322 122 40419
578	CAPACITOR,CHIP	220NF	10%	63V	5322 122 31999
579-581	CAPACITOR,CERAM	1NF	10%	63V	5322 122 40419
582	CAP.ELEC.SAL	15UF	10%	16V	4822 124 20977
583,586	CAPACITOR,CERAM	1NF	10%	63V	5322 122 40419
584	CAPACITOR,FOIL	1UF	5%	50V	5322 121 42398
585	CAP,ELEC.SAL	10UF	20%	16V	5322 124 14066
587,590	CAPACITOR,CERAM	100N	10%	50V	5322 122 32002
588,593	CAPACITOR,CHIP	220NF	10%	63V	5322 122 31999
589	CAPACITOR,CERAM	100NF	10%	50V	5322 122 32002
591	CAPACITOR,CERAM	1NF	10%	63V	5322 122 40418
592,597	CAPACITOR,CHIP	220NF	10%	63V	5322 122 31999
594	CAPACITOR,CERAM	56PF	2%	63V	5322 122 40408
595	CAPACITOR,TRIMM	20PF-2PF			4822 125 50201
596	CAPACITOR,CHIP	820PF	80%	400V	5322 122 32001
599	CAPACITOR,TRIMM	3-8PF			5322 125 60097

RESISTORS/RF-U1

ITEM	DESCRIPTION				ORDERING CODE
600	RESISTOR,CARBON	10E	5%	0,2W	4822 116 52176
625-628	RESISTOR,CARBON	16E	5%	0,2W	4822 111 30712
629,660	RESISTOR,CARBON	51E	5%	0,2W	4822 111 30769
638	POTM,TRIMMING	470E	LIN	0,5W	5322 101 14047
641,652	RESISTOR,CARBON	1K	5%	0,2W	4822 116 52204
649,733	RESISTOR,CARBON	150E	5%	0,2W	4822 111 30325
657,662	RESISTOR,CARBON	1K	5%	0,2W	4822 116 52204
664,666	RESISTOR,CARBON	1K	5%	0,2W	4822 116 52204
659	RESISTOR,CARBON	75E	5%	0,2W	4822 111 30787
667,668	RESISTOR,CARBON	150E	5%	0,2W	4822 111 30325
673,681	RESISTOR,CARBON	1K	5%	0,2W	4822 116 52204
678	RESISTOR,M.FILM	910E	5%	0,2W	4822 116 52232
680,697	RESISTOR,CARBON	51E	5%	0,2W	4822 111 30769
684	RESISTOR,CARBON	1K	5%	0,2W	4822 116 52204
687	RESISTOR,M.FILM	1E1	5%	0,33W	4822 110 70028
698	RESISTOR,CARBON	75E	5%	0,2W	4822 111 30787
699	RESISTOR,M.FILM	1E33	1%	0,4W	5322 116 51357
707	RESISTOR,CARBON	16E	5%	0,2W	4822 111 30712
708	RESISTOR,CARBON	51E	5%	0,2W	4822 111 30769
718	RESISTOR,CARBON	360E	5%	0,2W	4822 111 30746
724	RESISTOR,CARBON	560E	5%	0,2W	4822 116 52226
726,727	RESISTOR,CARBON	22E	5%	0,2W	4822 116 52186
728	RESISTOR,CARBON	56E	5%	0,2W	4822 116 52197
731	RESISTOR,CARBON	1K	5%	0,2W	4822 116 52204
735,737	RESISTOR,CARBON	100E	5%	0,2W	4822 111 30324
736*	RESISTOR,CARBON	75E	5%	0,2W	4822 111 30787

* may be altered in test

ITEM	DESCRIPTION				ORDERING CODE	
738	RESISTOR,M.FILM	100E	5%	0,2W	4822 116 52175	
740	RESISTOR,NTC	4K7		0,6W	4822 116 30021	

COILS/RF-U1

805,807	COIL	4,7UH	5322 158 10628
812,815	COIL	15UH	5322 158 10629
817,819	COIL	4,7UH	5322 158 10628
820,821	COIL	220UH	5322 158 14034
823	COIL	4,7UH	5322 158 10628
824	COIL	100UH	5322 158 20448

MIXER/RF-U1

851	DIODE	DB BAL.MIXER TFM4	5322 130 32168
852	DIODE	DB BAL.MIXER TFM2	5322 130 32167

RF UNIT 2

TRANSISTORS/RF-U2

351	TRANSISTOR	BF480	5322 130 44582
352	TRANSISTOR	BFR96/02	5322 130 44911
353	TRANSISTOR	BD677	4822 130 41484
354-360	TRANSISTOR	BC548B	4822 130 40937
361	TRANSISTOR	BCY79/VIII	5322 130 44908

DIODES/RF U2

401,402	DIODE	BAX12A	5322 130 34605
403	DIODE,REFERENCE	BZV46-C2VO	4822 130 31248
405	DIODE	BAW62	4822 130 30613
411,412	DIODE	BB909A	5322 130 32162
421	DIODE	BB405B	5322 130 34953
431	DIODE,REFERENCE	BZX79-B27	4822 130 34379

INTEGRATED CIRCUITS/RF-U2

301,302	INTEGR.CIRCUIT	OM350	5322 209 81008	
303	INTEGR.CIRCUIT	11C90DC	5322 209 85458	LO 07 onw.
304	INTEGR.CIRCUIT	MC10131P	5322 209 85802	
305	INTEGR.CIRCUIT	11C90DC	5322 209 85458	
306	INTEGR.CIRCUIT	OM350	5322 209 81008	
307	INTEGR.CIRCUIT	SP4541	5322 209 82348	
308	INTEGR.CIRCUIT	HEF4040BP	5322 209 14269	
309,310	INTEGR.CIRCUIT	HEF4071BP	5322 209 14053	
311	INTEGR.CIRCUIT	HEF4073BP	5322 209 14066	
312	INTEGR.CIRCUIT	MC4044L	5322 209 85821	
313	INTEGR.CIRCUIT	HEF4024BP	5322 209 14103	
314	INTEGR.CIRCUIT	HEF4750VD	5322 209 10524	
315	INTEGR.CIRCUIT	NE538N	5322 209 81343	
321	INTEGR.CIRCUIT	7905UC	5322 130 44843	
322	INTEGR.CIRCUIT	UA7805CU	5322 209 84841	
323	INTEGR.CIRCUIT	UA723CN	5322 209 85889	LO 06 onw.
323**	INTEGR.CIRCUIT	NE550N	5322 209 85797	unt.LO 05.
	** see info fig. 46			

CAPACITORS/RF-U2

481,482	CAP,FEEDTROUGH	2,2NF	80%	160V	5322 122 70114	
483-487	CAP,FEEDTROUGH	47PF	10%	160V	5322 122 70112	
488-495	CAP,FEEDTROUGH	2,2NF	80%	160V	5322 122 70114	
496	CAPACITOR,CERAM	100N	10%	50V	5322 122 32002	
501-502	CAPACITOR,CERAM	1NF	10%	63V	5322 122 40419	
503	CAPACITOR,CHIP	1NF	10%	63V	5322 122 31998	LO 04 onw.
504	CAPACITOR,CERAM	10PF	2%	63V	5322 122 40397	
505,506	CAPACITOR,CERAM	22PF	2%	63V	5322 122 40398	

* may be altered in test

ITEM	DESCRIPTION				ORDERING CODE	
507	CAPACITOR,CERAM	10PF	2%	63V	5322 122 40397	
508,511	CAPACITOR,CERAM	1NF	10%	100V	5322 122 40419	
509	CAPACITOR,CERAM	4,7NF	10%	100V	5322 122 30128	
510	CAP.ELECT.SAL	15UF	20%	16V	4822 124 20977	
512	CAP.ELECT.SAL	1UF	20%	25V	4822 124 20944	
513,514	CAPACITOR,CERAM	100N	10%	50V	5322 122 32002	
515	CAPACITOR,CHIP	1NF	10%	63V	5322 122 31998	LO 0 5 onw.
520	CAPACITOR,CERAM	22NF	80%	63V	5322 122 31795	
521,531	CAPACITOR,CERAM	15UF	10%	16V	4822 124 20977	
522	CAPACITOR,CERAM	18PF	2%	63V	5322 122 40409	
523	CAPACITOR,CHIP	820PF	80%	400V	5322 122 32001	
524	CAPACITOR,CERAM	2,7PF	0,25PF	63V	5322 122 40401	
525,532	CAPACITOR,CERAM	4,7NF	10%	100V	4822 122 30128	
533	CAPACITOR,CERAM	15PF	10%	400V	5322 122 40417	
534	CAPACITOR,CERAM	0,68PF	0,25PF	63V	5322 122 40411	
535,545	CAPACITOR,CERAM	100N	10%	50V	5322 122 32002	
536,541	CAPACITOR,CERAM	4,7NF	10%	100V	5322 122 30128	
540	CAPACITOR,CHIP	1NF	10%	63V	5322 122 31998	
542,543	CAPACITOR,CHIP	1NF	10%	63V	5322 122 31998	
546	CAPACITOR,CERAM	1NF	10%	63V	5322 122 40419	
544,547	CAPACITOR,CERAM	22NF	80%	63V	5322 122 31795	
548	CAPACITOR,CERAM	1NF	10%	63V	5322 122 40419	
549,551	CAPACITOR,CERAM	22NF	80%	63V	5322 122 31795	
550	CAP.ELECTROLYT.	100MU		50V	4822 124 21348	
552	CAPACITOR,FOIL	1UF	10%	50V	5322 121 41883	
553	CAP.ELECTROLYT.	2,2UF	50%	63V	4822 124 40244	
554-556	CAPACITOR,CERAM	22NF	80%	63V	5322 122 31795	
561	CAPACITOR,FOIL	220NF	10%	100V	4822 121 40232	
562	CAPACITOR,CERAM	12PF	2%	63V	5322 122 40404	
563	CAPACITOR,TRIMM	2,5-27P		100V	5322 125 54083	
564	CAPACITOR,CERAM	220PF	2%	63V	5322 122 40407	
565	CAPACITOR,CERAM	120PF	2%	63V	5322 122 40406	
566,567	CAPACITOR,CERAM	1NF	10%	63V	5322 122 40419	
570,571	CAPACITOR,CERAM	4,7NF	10%	100V	4822 122 30128	
572	CAPACITOR,CERAM	22NF	80%	63V	5322 122 31795	
573	CAPACITOR,FOIL	680PF	1%	250V	5322 121 54174	
574	CAPACITOR,FOIL	16NF	1%	160V	5322 121 50612	
575	CAPACITOR,FOIL	10NF	1%	63V	5322 121 54154	
576,577	CAP,ELECTROLYT.	200UF	50%	16V	4822 124 40196	
578	CAPACITOR,CERAM	100N	10%	50V	5322 122 32002	
579	CAPACITOR,FOIL	470NF			5322 121 41884	
580	CAPACITOR,CERAM	4,7NF	10%	100V	4822 122 30128	
581	CAPACITOR,CERAM	330PF	2%	100V	4822 122 31353	
591-593	CAP.ELECTROLYT.	220UF	50%	16V	4822 124 40196	
594	CAP,ELEC.SAL	4,7UF	20%	25V	4822 124 10367	
595	CAPACITOR,CERAM	470PF	10%	100V	5322 122 31796	
596	CAPACITOR,CHIP	1NF	10%	63V	5322 122 31998	
597	CAPACITOR,CERAM	12PF	2%	63V	5322 122 40404	

RESISTOR/RF-U2

604,616*	RESISTOR,CARBON	16E	5%	0,2W	4822 111 30712
605	RESISTOR,M.FILM	1E	1%	0,4W	4822 116 51179
608	RESISTOR,CARBON	75E	5%	0,2W	4822 111 30787
626*	RESISTOR,CARBON	16E	5%	0,2W	4822 111 30712
627	RESISTOR,CARBON	51E	5%	0,2W	4822 111 30769
632	RESISTOR,M.FILM	1E33	1%	0,4W	5322 116 51357
633	RESISTOR,CARBON	360E	5%	0,2W	4822 111 30746
637	RESISTOR-NETW.	5X47K	5%	0,125W	5322 116 90129
676	RESISTOR,HT	2,7M		0,2W	4822 110 72198
693	RESISTOR,CARBON	51E	5%	0,2W	4822 111 30769

* value may be altered in test

ITEM	DESCRIPTION				ORDERING CODE	
694	RESISTOR,CARBON	100E	5%	0,2W	4822 111 30324	
695	RESISTOR,CARBON	10E	5%	0,2W	4822 111 30347	
698	RESISTOR,CARBON	39E	5%	0,2W	4822 111 30069	LO 04 onw.
699	RESISTOR,M.FILM	24E	5%	0,2W	4822 116 52187	LO 04 onw.

CRYSTAL/RF-U2

751	CRYSTAL	5,00MHZ			5322 242 70718	

COILS/RF-U2

801	COIL	4,7UH			5322 158 10628	
805-808	COIL	15UH			5322 158 10629	
813	COIL	15UH			5322 158 10629	

MIXER/RF-U2

851	DIODE	DB BAL.MIXER TFM4			5322 130 32168	

CONNECTION BOARD RF, CAPACITORS

1-4	CAP,FEEDTROUGH	2,7NF	80%	160V	5322 122 70115	
5,8	CAP,FEEDTROUGH	47PF	10%	160V	5322 122 70113	
6,7	CAP,FEEDTROUGH	2,2NF	80%	160V	5322 122 70115	
13-16	CAP,FEEDTROUGH	2,2NF	80%	160V	5322 122 70115	
21,22	CAP,FEEDTROUGH	47PF	10%	160V	5322 122 70113	
23-33	CAP,FEEDTROUGH	2,2NF	80%	160V	5322 122 70115	
34-36	CAP,FEEDTROUGH	47PF	10%	160V	5322 122 70113	
40-43	CAP,ELEC.TANTAL	10UF	50%	16V	5322 124 14066	
532	CAP,ELECTRLYT.	68UF	50%	16V	4822 124 20689	
533	CAPACITOR,FOIL	470N	10%		5322 121 41884	

RF UNIT 10

DIODES/RF-U10

401,402	DIODE	BA244			5322 130 34794	

CAPACITORS/RF-U10

501,504	CAPACITOR,CERAM	18PF	2%	63V	5322 122 40421	
502,503	CAPACITOR,CERAM	39PF	2%	63V	5322 122 40422	

RF UNIT 1

DIODES/RF-U11

401,402	DIODE	BA244			5322 130 34794	

CAPACITORS/RF-U11

501,504	CAPACITOR,CERAM	10PF	2%	63V	5322 122 40397	
502,503	CAPACITOR,CERAM	18PF	2%	63V	5322 122 40421	
505	CAPACITOR,CHIP	1NF	10%	63V	5322 122 31998	

RESISTORS/RF-U11

601	RESISTOR,CARBON	1K	5%	0,2W	4822 116 52204	
602	RESISTOR,CARBON	39E	5%	0,2W	4822 111 30069	

POWER AMPLIFIER/RF,U12 (PM 5390S only)

INTEGRATED CIRCUITS/RF-U12

301,302	INTEGR.CIRCUIT	GPD331			5322 209 81781	
303	INTEGR.CIRCUIT	MWA330			5322 209 81782	
304	INTEGR.CIRCUIT	MWA320			5322 209 81778	

* value may be altered in test

ITEM	DESCRIPTION				ORDERING CODE	
DIODES/RF-U12						
401-404	DIODE	BA379			5322 130 80399	
405,406	DIODE	BAX12A			5322 130 34605	
CAPACITORS/RF-U12						
501-516	CAPACITOR,CHIP	220NF	10%	63V	5322 122 31999	
517-520	CAPACITOR,TRIMM	0,6-3,5PF		160V	5322 125 60098	
518,523	CAP.CHIP	220NF	10%	63V	5322 122 31999	LO 07 onw.
521	CAPACITOR,CERAM	1NF	10%	63V	5322 122 40419	LO 07 onw.
522,524	CAPACITOR,CHIP	OP68	0,25PF	63V	5322 122 40411	LO 07 onw.
530	CAP.FEEDTROUGH	FKE350			5322 121 44228	
RESISTORS/RF-U12						
601	RESISTOR,CHIP	4E7	10%	0,125W	5322 111 90376	
602,606	RESISTOR,CARBON	1K	5%	0,2W	4822 111 30269	
607	RESISTOR,M.FILM	1E78	1%	0,4W	5322 116 51755	
610,615	RESISTOR	1K	5%	0,2W	4822 111 30269	
619	RESISTOR,CARBON	16E	5%	0,2W	4822 111 30712	
620*	RESISTOR,CARBON	270E	5%	0,2W	4822 116 52217	
622,633*	RESISTOR,CARBON	360E	5%	0,2W	4822 111 30746	
624	RESISTOR,M.FILM	390E	5%	1,6W	4822 116 51104	
626*	RESISTOR,CARBON	39E	5%	0,2W	4822 111 30069	LO 05 onw.
631	RESISTOR,CARBON	220E	5%	0,2W	4822 111 30327	
632,634*	RESISTOR,CARBON	10E	5%	0,2W	4822 116 52176	

* value may be altered in test

LACQUERED METAL FILM RESISTORS MR25

style	resistance range	tol. ±%	series	temperature coefficient ±ppm/°C	limiting voltage (r.m.s.) V	service code no. 5322 116 5.... followed by
MR 25	4,99 Ω – 301 kΩ	1	E96	50 *	250	

* For resistance values lower than 49,9 Ω: 100 ppm/°C.

4,99	0568	16,5	4109	54,9	4445	182	4493	604	4528
5,11	4192	16,9	0627	56,2	4446	187	4494	619	4529
5,23	4113	17,4	4432	57,6	4447	191	4495	634	4531
5,36	4239	17,8	0418	59	4448	196	0676	649	4532
5,49	4102	18,2	4083	60,4	4449	200	4496	665	4533
5,62	4128	18,7	0895	61,9	4451	205	0669	681	4534
5,76	4413	19,1	4104	63,4	4375	210	4036	698	4037
5,90	1064	19,6	0473	64,9	4453	215	0457	715	0571
6,04	4114	20	1048	66,5	4454	221	4002	732	4535
6,19	1049	20,5	0678	68,1	4455	226	4497	750	4536
6,34	0862	21	4433	69,8	4456	232	4498	768	4537
6,49	4112	21,5	0677	71,5	4457	237	0679	787	4538
6,65	4414	22,1	0983	73,2	4458	243	0437	806	4539
6,81	4013	22,6	0491	75	4459	249	4499	825	4541
6,98	4103	23,2	4434	76,8	0494	255	4501	845	4542
7,15	4415	23,7	4014	78,7	0578	261	4502	866	4543
7,32	4416	24,3	4435	80,6	4461	267	4503	887	4544
7,50	4417	24,9	0903	82,5	4462	274	4504	909	4545
7,68	4418	25,5	4436	84,5	4463	280	4505	931	4546
7,87	4046	26,1	0876	86,6	4464	287	4506	953	4547
8,06	4419	26,7	4067	88,7	4465	294	4507	976	4548
8,25	4099	27,4	0493	90,9	4466	301	4508	1K	4549
8,45	4421	28	0623	93,1	4467	309	4509	1K02	4551
8,66	1051	28,7	4068	95,3	0569	316	4511	1K05	4552
8,87	4101	29,4	4084	97,6	4468	324	4512	1K07	4553
9,09	0863	30,1	0904	100	4469	332	4513	1K1	4554
9,31	4422	30,9	4437	102	4471	340	4514	1K13	4555
9,53	4258	31,6	4034	105	4472	348	4515	1K15	0415
9,76	4423	32,4	4105	107	4473	357	0603	1K18	4556
10	0452	33,2	0527	110	4474	365	4516	1K21	4557
10,2	4111	34	4438	113	4475	374	4517	1K24	4559
10,5	4071	34,8	4027	115	4476	383	4518	1K27	0555
10,7	4424	35,7	4439	118	4477	392	4006	1K3	0526
11	4059	36,5	0409	121	4426	402	4519	1K33	4561
11,3	4425	37,4	4158	124	4478	412	4521	1K37	0628
11,5	0838	38,3	0954	127	4479	422	0459	1K4	4562
11,8	0738	39,2	4087	130	4481	432	4522	1K43	4563
12,1	4069	40,2	0926	133	4482	442	0592	1K47	0635
12,4	4427	41,2	4108	137	4483	453	4523	1K5	4564
12,7	4261	42,2	1052	140	4484	464	0536	1K54	0586
13	4082	43,2	0519	143	4485	475	4007	1K58	0622
13,3	1047	44,2	0818	147	0766	487	0508	1K62	4565
13,7	4428	45,3	0795	150	4486	499	4524	1K65	4566
14	0839	46,4	0492	154	0506	511	4525	1K69	4567
14,3	4429	47,5	0952	158	4487	523	4526	1K74	0629
14,7	0412	48,7	0511	162	0417	536	0621	1K78	5015
15	0902	49,9	4441	165	4488	549	0732	1K82	4568
15,4	0925	51,1	4442	169	4489	562	4009	1K87	0728
15,8	0861	52,3	4443	174	4491	576	4527	1K91	4569
16,2	4431	53,6	4444	178	4492	590	0561	1K96	4571

2K	4572	6K65	4604	22K1	4003	73K2	0666	243K	4733
2K05	0664	6K81	4012	22K6	0481	75K	4686	249K	4734
2K1	4573	6K98	4605	23K2	4645	76K8	4687	255K	4735
2K15	0767	7K15	4606	23K7	4646	78K7	0533	261K	4736
2K21	4574	7K32	4607	24K3	4647	80K6	4688	267K	4737
2K26	0675	7K5	4608	24K9	4648	82K5	4689	274K	4738
2K32	4575	7K68	4609	25K5	4649	84K5	4691	280K	4739
2K37	4576	7K87	0458	26K1	4651	86K6	4692	287K	4741
2K43	4004	8K06	4611	26K1	4652	88K7	4693	294K	4742
2K49	0581	8K25	4558	27K4	0559	90K9	4694	301K	4743
2K55	4577	8K45	4612	28K	0667	93K1	4297	316 K	5268
2K61	0671	8K66	4613	28K7	4653	95K3	0567	332 K	1184*
2K67	4578	8K87	4614	29K4	4654	97K6	4695	348 K	5499
2K74	0636	9K09	4615	30K1	4655	100K	4696	365 K	5641
2K8	4579	9K31	4616	30K9	4656	102K	4697	374 K	5457
2K87	0414	9K53	4617	31K6	4657	105K	4698	383 K	5335
2K94	4581	9K76	4618	32K4	4658	107K	4699	402 K	5283
3K01	0524	10K	4619	33K2	0482	110K	4701	412 K	5424
3K09	4582	10K2	4621	34K	4659	113K	4702	422 K	5247
3K16	0579	10K5	0731	34K8	4661	115K	4279	442 K	5458
3K24	4583	10K7	4622	35K7	4662	118K	4703	464 K	5207
3K32	4005	11K	4623	36K5	0726	121K	4704	475 K	1275
3K4	4584	11K3	0668	37K4	4663	124K	4705	499 K	5468
3K48	4585	11K5	4624	38K3	0483	127K	4706	511 K	5258
3K57	4586	11K8	4625	39K2	4664	130K	4707	536 K	4758
3K65	4587	12K1	0572	40K2	4665	133K	4708	562 K	1169
3K74	4588	12K4	4626	41K2	4666	137K	4709	590 K	5567
3K83	4589	12K7	0443	42K2	0474	140K	4259	619 K	5315
3K92	4591	13K	0522	43K2	4667	143K	4711	649 K	5331
4K02	4592	13K3	4627	44K2	4668	147K	4712	681 K	5284
4K12	4593	13K7	4628	45K3	4669	150K	4713	750 K	5532
4K22	0729	14K	4629	46K4	0557	154K	4714	806 K	1369
4K32	4594	14K3	4631	47K5	4671	158K	4715	825 K	1398
4K42	0556	14K7	4632	48K7	0442	162K	4716	866 K	1395
4K53	0631	15K	4001	49K9	0674	165K	4717	909 K	5533
4K64	0484	15K4	0479	51K1	0672	169K	4718	953 K	1368
4K75	4008	15K8	4633	52K3	4673	174K	4719	1MAO	5535
4K87	0509	16K2	0593	53K6	4674	178K	4721		
4K99	0523	16K5	4634	54K9	4675	182K	4722		
5K11	4595	16K9	4635	56K2	4676	187K	4723		
5K23	4596	17K4	4636	57K6	4677	191K	4724		
5K36	4597	17K8	4637	59K	4678	196K	4725		
5K49	4598	18K2	4638	60K4	4679	200K	4726		
5K62	4011	18K7	0558	61K9	0872	205K	4727		
5K76	4599	19K1	4639	63K4	4681	210K	4208		
5K9	0583	19K6	4641	64K9	0514	215K	4728		
6K04	4601	20K	4642	66K5	4682	221K	4038		
6K19	0608	20K5	4643	68K1	4683	226K	4729		
6K34	4602	21K	4644	69K8	4684	232K	4731		
6K49	4603	21K5	0451	71K5	4685	237K	4732		

* 4822 116 5 . . .

FREQUENCY SYNTHESIZER

HEF4750V

LSI

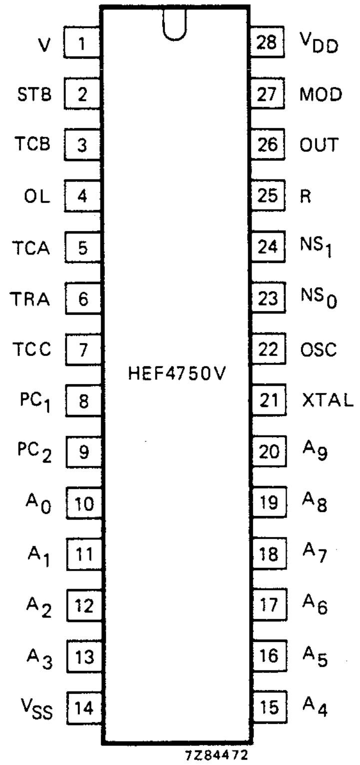


Fig. 1 Pinning diagram.

HEF4750VD: 28-lead DIL; ceramic (cerdip) (SOT-135A).

PINNING

R	phase comparator input, reference
V	phase comparator input
STB	strobe input
TCA	timing capacitor C_A pin
TCB	timing capacitor C_B pin
TCC	timing capacitor C_C pin
TRA	biasing pin (resistor R_A)
PC_1	analogue phase comparator output
PC_2	digital phase comparator output
MOD	phase modulation input
OL	out-of-lock indication
OSC	reference oscillator/buffer input
XTAL	reference oscillator/buffer output
A_0 to A_9	programming inputs/programmable divider
NS_0, NS_1	programming inputs, prescaler
OUT	reference divider output

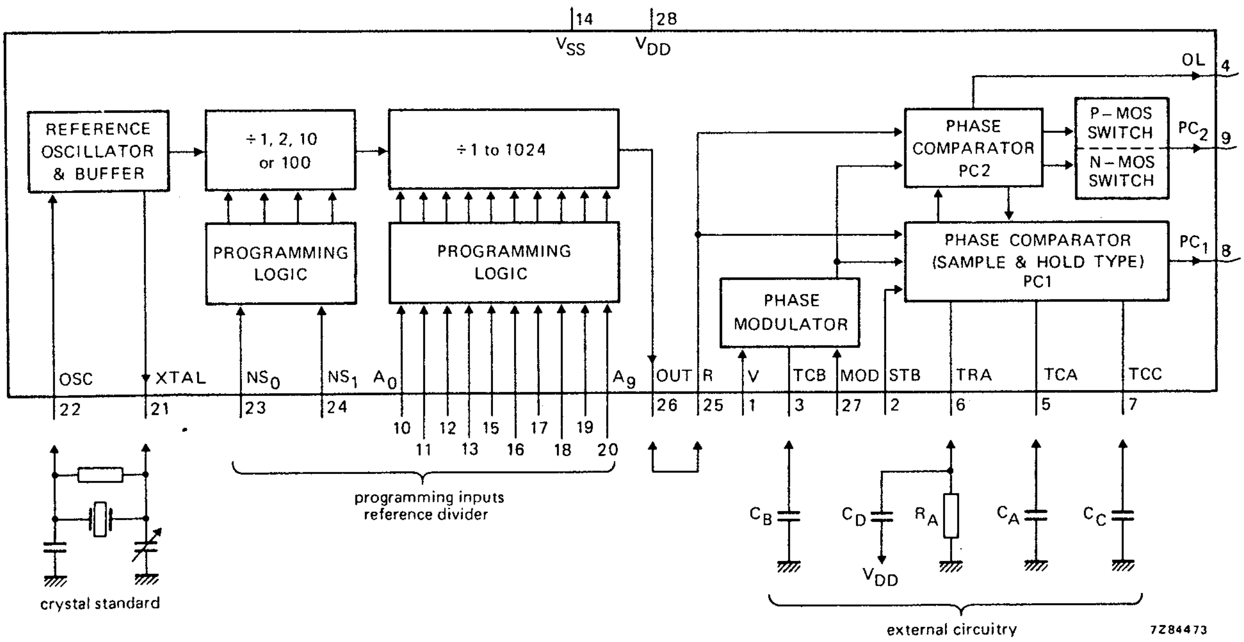


Fig. 2 Block diagram comprising five basic functions: phase comparator 1 (PC1), phase comparator 2 (PC2), phase modulator, reference oscillator and reference divider. These functions are described separately.

N.B. PC_1 = analogue output; PC_2 = 3-state output.

UNIVERSAL DIVIDER

The HEF4751V is a universal divider (U.D.) intended for use in high performance phase lock loop frequency synthesizer systems. It consists of a chain of counters operating in a programmable feedback mode. Programmable feedback signals are generated for up to three external (fast) ÷10/11 prescaler.

The system comprising one HEF4751V U.D. together with prescalers is a fully programmable divider with a maximum configuration of: 5 decimal stages, a programmable mode M stage ($1 \leqslant M \leqslant 16$, non-decimal fraction channel selection), and a mode H stage (H = 1 or 2, stage for half channel offset). Programming is performed in BCD code in a bit-parallel, digit-serial format.
To accommodate fixed or variable frequency offset, two numbers are applied in parallel, one being subtracted from the other to produce the internal programme.
The decade selection address is generated by an internal programme counter which may run continuously or on demand. Two or more universal dividers can be cascaded, each extra U.D. (in slave mode) adds two decades to the system. The combination retains the full programmability and features of a single U.D.
The U.D. provides a fast output signal FF at output OFF, which can have a phase jitter of ± 1 system input period, to allow fast frequency locking. The slow output signal FS at output OFS, which is jitter-free, is used for fine phase control at a lower speed.

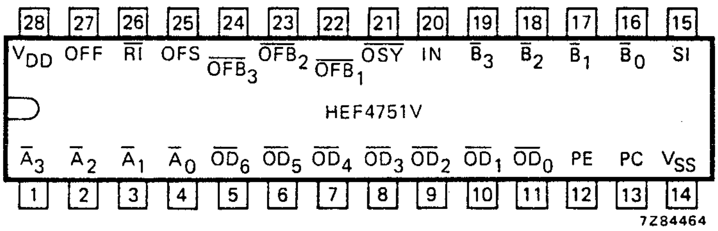


Fig. 1 Pinning diagram.

SUPPLY VOLTAGE

rating	recommended operating
−0,5 to +18	4,5 to 12,5 V

HEF4751VP : 28-lead DIL; plastic (SOT-117).
HEF4751VD: 28-lead DIL; ceramic (cerdip) (SOT-135A).
HEF4751VT : 28-lead mini-pack; plastic (SO-28; SOT-136A).

FAMILY DATA
I_{DD} LIMITS category LSI } see Family Specifications

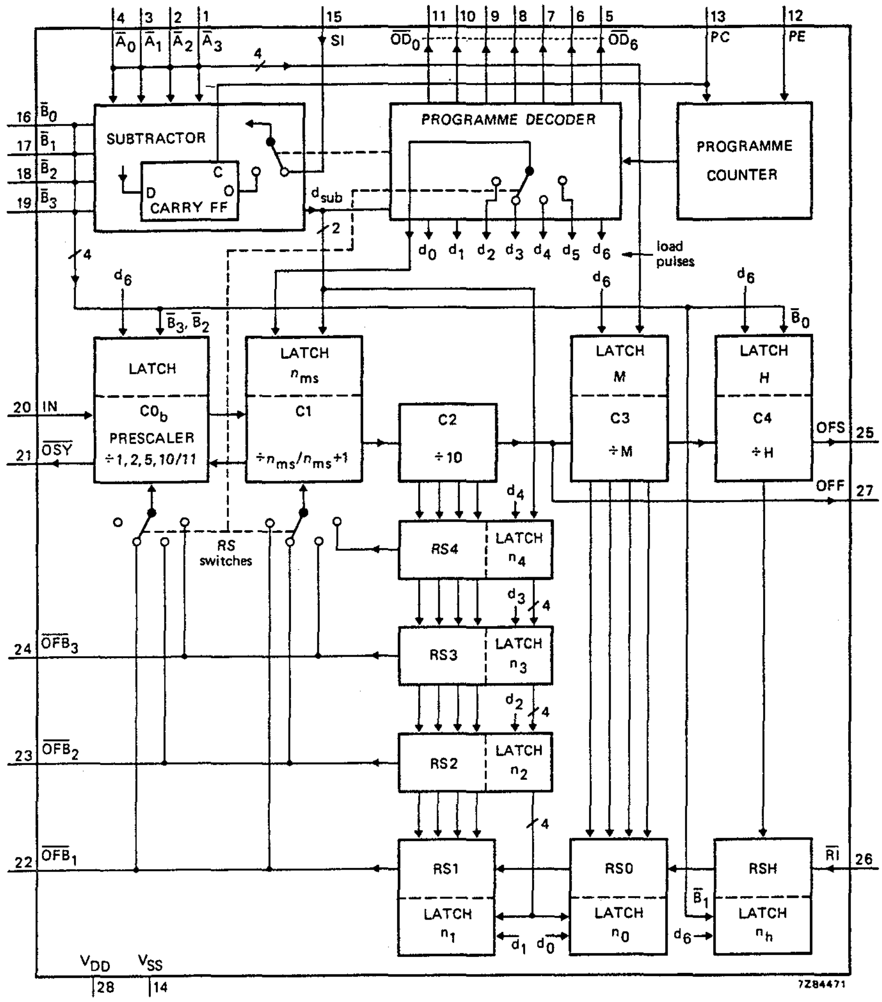


Fig. 2 Block diagram.

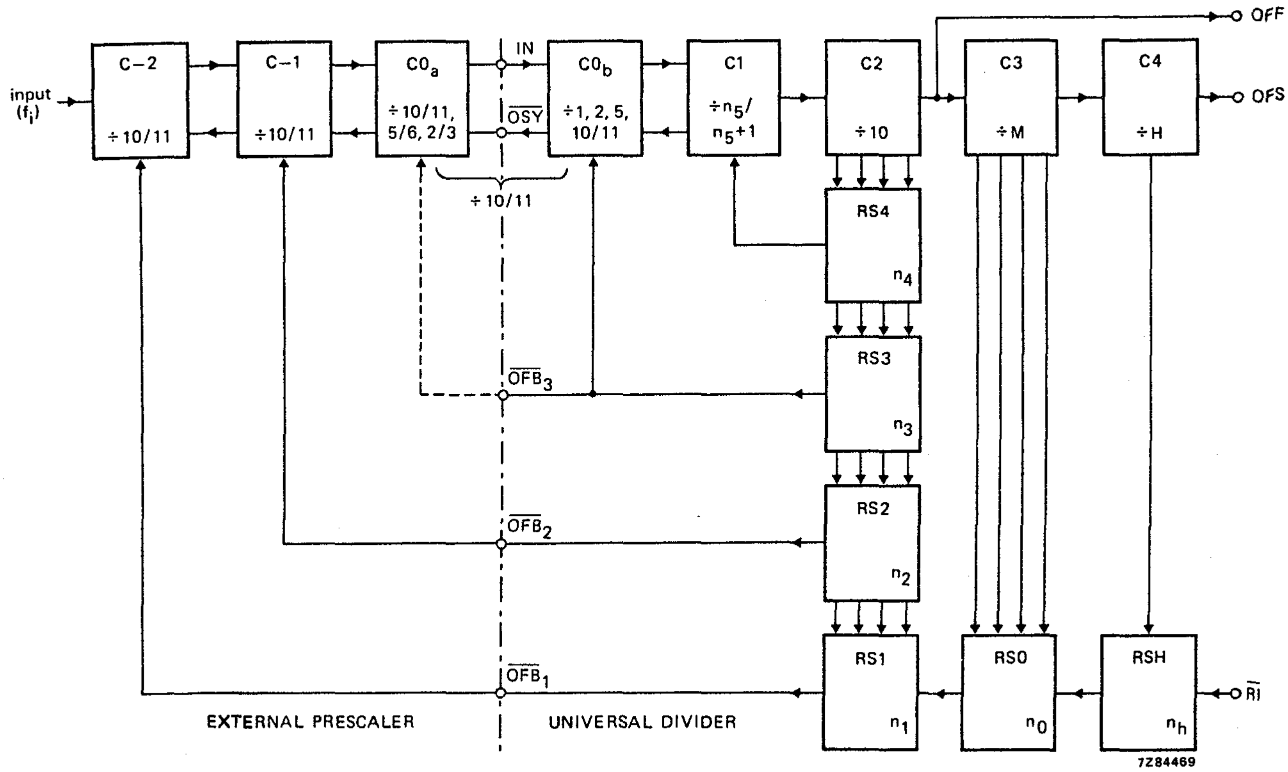


Fig. 3 The HEF4751V U.D. used in a system with 3 (fast) prescalers.
$1 \leqslant M \leqslant 16$; $1 \leqslant H \leqslant 2$; $n_5 > 0$; $f_i/f_{OFS} = \{(n_5 \cdot 10^4 + n_4 \cdot 10^3 + n_3 \cdot 10^2 + n_2 \cdot 10 + n_1)\, M + n_0\}\, H + n_h$.

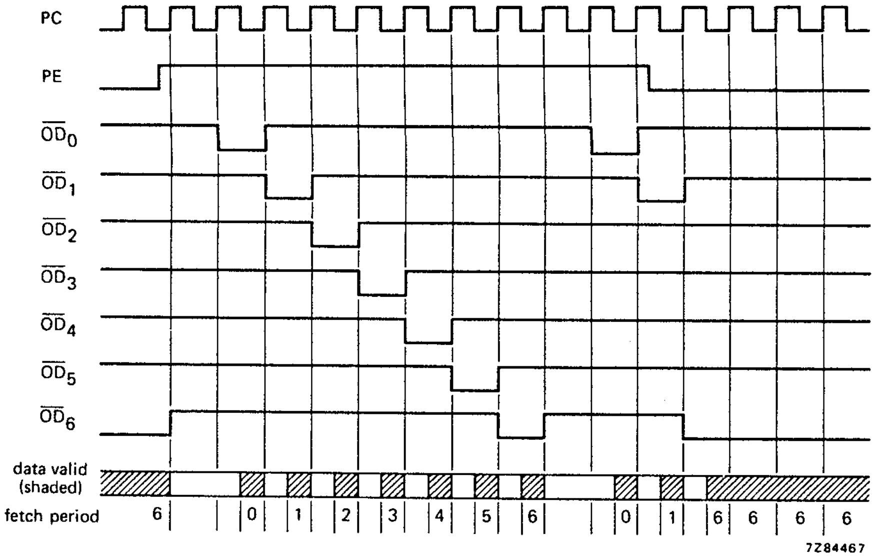


Fig. 4 Timing diagram showing programme data inputs.

Allocation of data input

fetch period	inputs		
	$\overline{A}_3$ $\overline{A}_2$ $\overline{A}_1$ $\overline{A}_0$	$\overline{B}_3$ $\overline{B}_2$ $\overline{B}_1$ $\overline{B}_0$	SI
0	n_{0A}	n_{0B}	b_{in}
1	n_{1A}	n_{1B}	X
2	n_{2A}	n_{2B}	X
3	n_{3A}	n_{3B}	X
4	n_{4A}	n_{4B}	X
5	n_{5A}	n_{5B}	X
6	M	CO_b control / ½ channel control	X

Allocation of data input $\overline{B}_3$ to $\overline{B}_0$ during fetch period 6

$\overline{B}_3$	$\overline{B}_2$	CO_b division ratio
L	L	1
L	H	2
H	L	5
H	H	10/11

$\overline{B}_1$	$\overline{B}_0$	½ channel configuration
L	L	H = 1
L	H	H = 2; $n_h = 0$
H	H	H = 2; $n_h = 1$
H	L	test state

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

PROGRAMME DATA INPUT (see also Figs 3 and 4)

The programming process is timed and controlled by input PC and PE. When the programme enable (PE) input is HIGH, the positive edges of the programme clock (PC) signal step through the internal programme counter in a sequence of 8 states. Seven states define fetch periods, each indicated by a LOW signal at one of the corresponding data address outputs ($\overline{OD}_0$ to $\overline{OD}_6$). These data address signals may be used to address the external programme source. The data fetched from the programme source is applied to inputs $\overline{A}_0$ to $\overline{A}_3$ and $\overline{B}_0$ to $\overline{B}_3$. When PC is LOW in a fetch period an internal load pulse is generated, the data is valid during this time and has to be stable. When PE is LOW, the programming cyclus is interrupted on the first positive edge of PC. On the next negative edge at input PC fetch period 6 is entered. Data may enter asynchronously in fetch period 6.

Ten blocks in the U.D. need programme input signals (see Fig. 2). Four of these (CO_b, C3, C4 and RSH) are concerned with the configuration of the U.D. and are programmed in fetch period 6. The remaining blocks (RS0 to RS4 and C1) are programmed with number P, consisting of six internal digits n_0 to n_5.

$P = (n_5 \cdot 10^4 + n_4 \cdot 10^3 + n_3 \cdot 10^2 + n_2 \cdot 10 + n_1) \cdot M + n_0$

These digits are formed by a substractor from two external numbers A and B and a borrow-in (b_{in}).

$P = A - B - b_{in}$ or if this result is negative; $P = A - B - b_{in} + M \cdot 10^5$.

The numbers A and B, each consisting of six four bit digits n_{0A} to n_{5A} and n_{0B} to n_{5B}, are applied in fetch period 0 to 5 to the inputs $\overline{A}_0$ to $\overline{A}_3$ (data A) and $\overline{B}_0$ to $\overline{B}_3$ (data B) in binary coded negative logic.

$A = (n_{5A} \cdot 10^4 + n_{4A} \cdot 10^3 + n_{3A} \cdot 10^2 + n_{2A} \cdot 10 + n_{1A}) \cdot M + n_{0A}$.

$B = (n_{5B} \cdot 10^4 + n_{4B} \cdot 10^3 + n_{3B} \cdot 10^2 + n_{2B} \cdot 10 + n_{1B}) \cdot M + n_{0B}$.

Borrow-in (b_{in}) is applied via input SI in fetch period 0 (SI = HIGH: borrow, SI = LOW: no borrow).

Counter C1 is automatically programmed with the most significant non-zero digit (n_{ms}) from the internal digits n_5 to n_2 of number P. The counter chain C – 2 to C1 (see Fig. 3) is fully programmable by the use of pulse rate feedback.

Rate feedback is generated by the rate selectors RS4 to RS0 and RSH, which are programmed with digits n_4 to n_0 and n_h respectively. In fetch period 6 the fractional counter C3, half channel counter C4 and CO_b are programmed and configured via data B inputs. Counter C3 is programmed in fetch period 6 via data A inputs in negative logic (except all HIGH is understood as: M = 16). The counter CO is a side steppable 10/11 counter composed of an internal part CO_b and an external part CO_a. CO_b is configured via $\overline{B}_3$ and $\overline{B}_2$ to a division ratio of 1 or 2 or 5 or 10/11; CO_a must have the complementary ratio 10/11 or 5/6 or 2/3 or 1 respectively. In the latter case CO_b comprises the whole CO counter with internal feedback, CO_a is then not required.

The half channel counter C4 is enabled with $\overline{B}_0$ = HIGH and disabled with $\overline{B}_0$ = LOW. With C4 enabled, a half channel offset can be programmed with input $\overline{B}_1$ = HIGH, and no offset with $\overline{B}_1$ = LOW.

11C90 10/11 PRESCALER

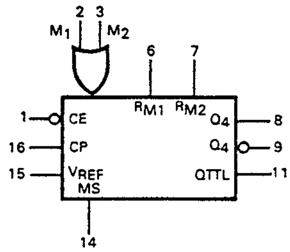
GENERAL DESCRIPTION – The 11C90 is a high speed prescaler designed specifically for communication and instrumentation applications. It will divide by either 10 or 11 over a frequency range from dc to typically 650 MHz. The division ratio is controlled by the mode control. The divide by 10 or 11 capability allows the use of pulse swallowing techniques to control high speed counting modulos by lower speed circuits. The 11C90 may be used with either ECL or TTL power supplies.

In addition to the ECL outputs $\overline{Q_4}$ and Q_4, the 11C90 contains an ECL-to-TTL converter and a TTL output. The TTL output operates from the same V_{CC} and V_{EE} levels as the counter, but a separate pin is used for the TTL circuit V_{EE}. This minimizes noise coupling when the TTL output switches and also allows power consumption to be reduced by leaving the separate V_{EE} pin open if the TTL output is not used.

To facilitate capacitive coupling of the clock signal, a 400 Ω resistor (V_{REF}) is connected internally to the V_{BB} reference. Connecting this resistor to the Clock Pulse input (CP) automatically centers the input signal about the switching threshold. Maximum frequency operation is achieved with a 50% duty cycle.

Each of the Mode Control inputs is connected to an internal 2 k resistor with the other end uncommitted (RM_1 and RM_2). An M input can be driven from a TTL circuit operating from the same V_{CC} by connecting the free end of the associated 2 k resistor to V_{CCA}. When an M input is driven from an ECL circuit, the 2 k resistor can be left open or, if required, can be connected to V_{EE} to act as a pull-down resistor. The device is packaged in a hermetic 16-pin ceramic Dual In-line package. It is available in commercial and military temperature ranges.

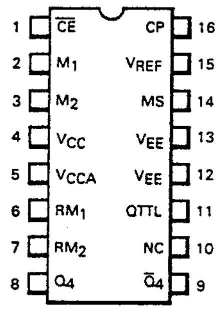
LOGIC SYMBOL



V_{CC} = Pin 4
V_{CCA} = Pin 5
V_{EE} = Pin 12
V_{EE} (TTL) = Pin 13

- VERY HIGH SPEED – 650 MHz TYPICAL
- DIVIDE BY 10/11 MODE CONTROL
- OPERATES FROM TTL OR ECL POWER SUPPLY
- HIGH SPEED TOTEM POLE TTL OUTPUT – 20 mA FAN-OUT
- COMPLEMENTARY ECL OUTPUTS DRIVE 50 Ω LINES
- SEPARATE TTL GND (V_{EE}) PIN MINIMIZES NOISE COUPLING
- PULL-UP RESISTORS ON MODE CONTROL INPUTS FOR TTL COMPATIBILITY
- INTERNAL BIASING REFERENCE FOR AC COUPLED CLOCKING
- INTERNAL 50 kΩ INPUT PULL-DOWNS – UNUSED INPUTS MAY BE LEFT OPEN
- COUNT ENABLE CONTROL FOR GATED CLOCKING
- ASYNCHRONOUS MASTER SET FOR INITIALIZING

CONNECTION DIAGRAM
DIP (TOP VIEW)

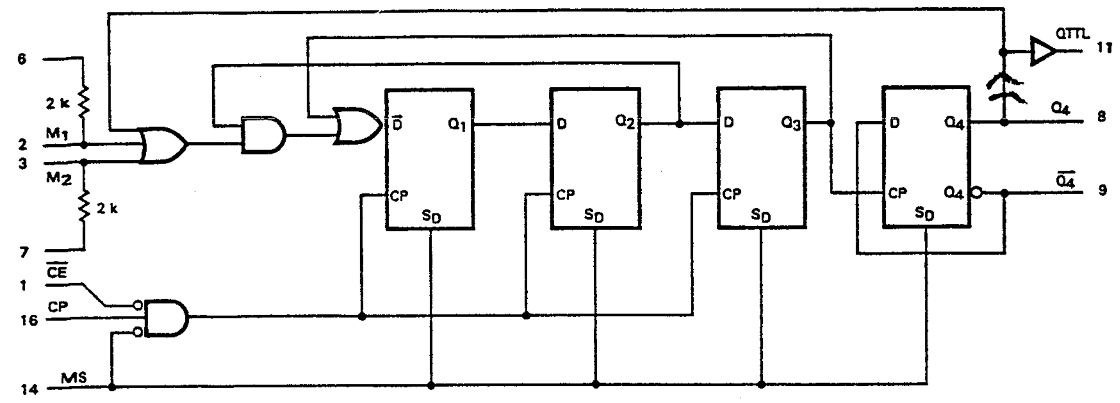


PIN NAMES

$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input
M_n	Count Modulus Control Input
MS	Asynchronous Master Set Input
Q_4, $\overline{Q_4}$	Complementary ECL Outputs
QTTL	TTL Output
RM_n	2 k Resistor to M_n
V_{REF}	400 Ω Resistor to V_{BB}

FAIRCHILD ECL • 11C90

LOGIC DIAGRAM



NOTE: This diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many internal functions are achieved more efficiently than shown.

FUNCTIONAL DESCRIPTION – The 11C90 contains four ECL flip-flops, an ECL to TTL converter and a Schottky TTL output buffer with an active pull-up. Three of the flip-flops operate as a synchronous shift counter driving the fourth flip-flop operating as an asynchronous toggle. The internal feedback logic is such that the TTL output and the Q_4 ECL output are HIGH for six clock periods and LOW for five clock periods. The Mode Control (M) inputs can modify the feedback to make the output HIGH for five clock periods and LOW for five clock periods, as indicated in the Count Sequence Table.

The feedback logic is such that at the instant the output goes HIGH, the circuit is already committed as to whether the output period will be 10 or 11 clock periods long. This means that subsequent changes in an M input signal, including decoding spikes, will have no effect on the current output period. The only timing restriction for an M input signal is that it be in the desired state at least a set-up time before the clock that follows the HHLL state shown in the table. The allowable propagation delay through external logic to an M input is maximized by designing it to use the positive transition of the 11C90 output as its active edge. This gives an allowable delay of ten clock periods, minus the CP to Q delay of the 11C90 and the M to CP set-up time. If the external logic uses the negative output transition as its active edge, the allowable delay is reduced to five clock periods minus the aforementioned delay and set-up time.

Capacitively coupled triggering is simplified by the 400 Ω resistor which connects pin 15 to the internal V_{BB} reference. By connecting this to the CP input, as shown in *Figure a*, the clock is automatically centered about the input threshold. A clock duty cycle of 50% provides the fastest operation, since the flip-flops are master/slave types with offset clock thresholds between master and slave. This feature ensures that the circuit will operate with clock waveforms having very slow rise and fall times, and thus, there is no minimum frequency restriction. Recommended minimum and maximum clock amplitude as a function of a frequency and temperature are shown in the graph labeled *Figure e*. When the CP or any other input is driven from another ECL circuit, normal ECL termination methods are recommended. One method is indicated in *Figure b*. Other ECL termination methods are discussed in the Fairchild ECL Handbook, Chapters 4 and 5.

When an M input is to be driven from a TTL output operating from the same V_{CC} and ground (V_{EE}), the internal 2 k resistor can be used to pull the TTL output up as shown in *Figure c*. Some types of TTL outputs will only pull up to within two diode drops of V_{CC}, which is not high enough for 11C90 inputs. The resistor will pull the signal up through the threshold region, although this final rise may be somewhat slow, depending on wiring capacitance. A resistor network that gives faster rise and also lower impedance is shown in *Figure d*.

The ECL outputs have no pull-down resistors and can drive series or parallel terminated transmission lines. For short interconnections that do not require impedance matching, a 270 Ω to 510 Ω resistor to V_{EE} can be used to establish the V_{OL} level. Both V_{CC} pins must always be used and should be connected together as close to the package as possible. Pin 12 must always be connected to the V_{EE} side of the supply, while pin 13 is required only if the TTL output is used. Low impedance V_{CC} and V_{EE} distribution and rf bypass capacitors are recommended to prevent crosstalk with other circuits.

COUNT SEQUENCE TABLE

	Q_1	Q_2	Q_3	Q_4(QTTL)	
	H	H	H	H	◄ ÷ 11
÷ 10 ►	L	H	H	H	
	L	L	H	H	
	L	L	L	H	
	H	L	L	H	
	H	H	L	H	
	L	H	H	L	
	L	L	H	L	
	L	L	L	L	
	H	L	L	L	
	H	H	L	L	

Note: A HIGH on MS forces all Qs HIGH.

OPERATING MODE TABLE

INPUTS				OUTPUT
MS	$\overline{CE}$	M_1	M_2	RESPONSE
H	X	X	X	Set HIGH
L	H	X	X	Hold
L	L	L	L	÷ 11
L	L	H	X	÷ 10
L	L	X	H	÷ 10

X = Immaterial

MAKING PROGRAMMABLE UHF COUNTERS WHEN NONE ARE AVAILABLE OR . . . PULSE SWALLOWING REVISITED

(Reprinted from *Fairchild Journal of Semiconductor Progress*, Vol 3, No. 4)

Recent developments have aroused greater interest in VHF and UHF counters for applications such as mobile communications and digitally tuned FM and TV receivers. Along with such new applications, of course, comes the need for suitable test instruments and signal generators. Although these applications differ in many ways, they have one thing in common —the need for high speed programmable counters. However, it seems inevitable that for some applications the available programmable counters are not fast enough; or, the counters that are fast enough lack the programming capability. One way of getting around this dilemma is to combine the talents of a high speed counter with those of a programmable counter. *Figure 1* shows such a combination, with a UHF prescaler and a programmable counter (the "units" decade) cooperating in a pulse swallowing* scheme to simulate a programmable UHF decade.

Pulse swallowing has been described as a way of combining a counter that is very fast, but rather dumb, with a counter that is very smart, but rather slow, to make the rest of the logic think that there is a very fast, very smart counter up front. For purposes of discussion, a smart counter is defined as one that is fully programmable and directly or indirectly satisfies a few other requirements. Examples are the 10010/16 and 95010/16 ECL circuits and the 93S10/16 TTL elements illustrated in *Figure 2*. Each circuit has a Terminal Count (TC) output which is normally in the inactive state and goes to the active state (LOW for ECL, HIGH for TTL) when the circuit reaches its maximum count, and stays active as long as the circuit retains the maximum count. Each circuit has an active-LOW Parallel Enable ($\overline{PE}$) input and individual Preset data (P_n) inputs for the four flip-flops. A LOW signal on $\overline{PE}$ inhibits counting and enables synchronous presetting. A Count Enable (CE) input can prevent counting but cannot prevent presetting. Thus the synchronous operating modes of these circuits are Count Up, Hold and Preset, all of which are utilized in either a straightforward programmable counter or in a pulse swallowing counter. The built-in flexibility of these circuits is at the expense of speed, due to the auxiliary gating, the full synchronism, and the time required to do the housekeeping.

Figure 3 illustrates a conventional divider using the fully programmable circuits. The TC output of the first decade is designated f_2 and gates the f_1 pulses into the second stage. The TC of the second stage is the final output f_3 and also the PE signal for both stages. Following a Preset, the first stage produces an f_2 pulse (one f_1 period wide) after the first K pulses of f_1 and thereafter produces one f_2 pulse for every 10 f_1 pulses. The second stage, which could as easily be two or more decades, produces an output pulse for every 10 pulses of f_2. Treated as a system building block, the overall divide ratio N can be expressed as follows.

$$N = K + 10(M) \tag{1}$$

For changing the overall divide ratio, K can be considered a fine adjustment and M a course adjustment; therefore, the change in N due to changes in K and M is

$$\Delta N = \Delta K + 10(\Delta M) \tag{2}$$

The fixed ratio counter or prescaler is at the high end of the speed scale, but at the low end of the intelligence scale. *Figure 4* illustrates a fixed prescaler driving a programmable counter. The fixed prescaler takes away some of the flexibility in choosing the overall divide ratio N and in the fine adjustment of N, as shown in *Equations 3* and *4*.

$$N = P \bullet M \tag{3}$$

$$\Delta P = 0$$

$$\therefore \Delta N = P(\Delta M) \tag{4}$$

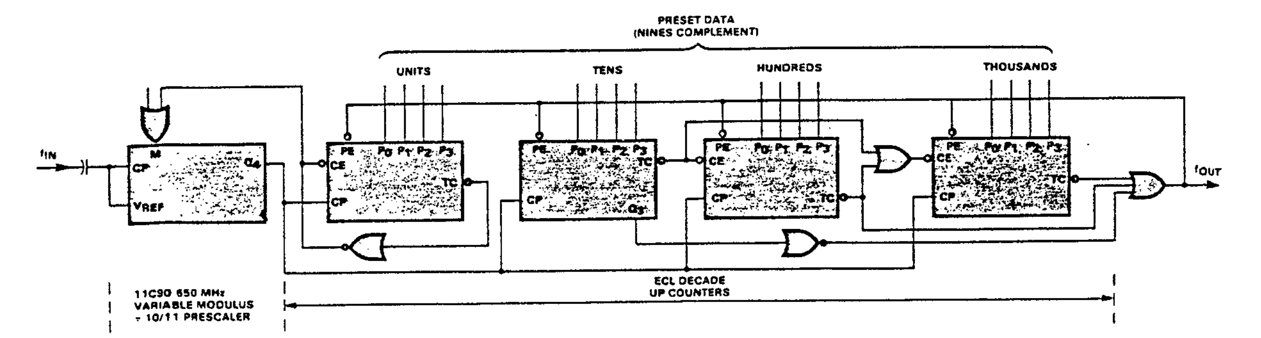


Fig. 1. 650 MHz Programmable Pulse Swallowing Counter

*Nichols, J. and Shinn, C., "Pulse Swallowing", EDN, October 1, 1970.

FAIRCHILD ECL • 11C90

While fully programmable counters offer a choice of 9 or 15 different divide ratios, the fixed prescaler offers only one choice. In between these two extremes is the variable modulus prescaler, in which a little bit of speed is sacrificed in favor of a little freedom in choosing divide ratios. A prescaler of this type plays a leading role in a pulse swallowing counter. An example is the 650 MHz 11C90 ÷ 10/11 prescaler shown symbolically in *Figure 5*.

The 11C90 contains three ECL flip-flops operating as a synchronous shift counter, driving a fourth ECL flip-flop operating as an asynchronous toggle. A shift counter is used because it is the fastest configuration in the synchronous menagerie. As a concession to speed, there are no preset inputs and only the outputs of the fourth flip-flop are brought out of the package. A third output repeats the Q waveform via an internal converter and a high speed totem-pole TTL buffer. The internal feedback logic is such that the output is HIGH for six cycles and LOW for five cycles of the input clock. An auxiliary input can modify the feedback so that the output is HIGH for five cycles and LOW for five cycles. In either case, at the instant the output goes HIGH, the circuit is already committed as to whether the output period will be 10 or 11 clock cycles long. Further, the decision as to the length of the next output period need not be made until just before the final (10th or 11th) clock of the current period. This feature means that any external logic operating with the 11C90 has almost 10 (or 11) clock periods in which to decide what the divide ratio of the next output period will be and apply the appropriate signal to the auxiliary control input.

A highly simplified block diagram of a pulse swallowing counter is shown in *Figure 6*. The variable modulus prescaler is shown as two fixed prescalers with a switch to select the output of either one. A swallow counter controls the position of the switch, while a program counter provides the net output f_3, which also serves as a Preset control. At the beginning of a cycle, the switch selects the upper prescaler. After S pulses of f_2, the swallow counter throws the switch to the lower prescaler output. Still later, the program counter reaches maximum and causes a Preset. This in turn causes the swallow counter to throw the switch back to the upper prescaler output and start a new cycle.

A slightly more sophisticated block diagram of a pulse swallowing counter is shown in *Figure 7*. The prescaler and the swallow counter are each one stage, while the program counter is normally two or more stages. As a starting point, assume that a parallel enable signal has just occurred and the preset data has been synchronously entered into all the counter flip-flops. This action returns the two TC outputs to the inactive state, ending the Preset mode. The TC signal of the swallow counter enables its CE input and changes the prescaler to the upper (numerically larger) divide ratio. Both counters start counting up, and after S pulses of f_2 the swallow counter reaches maximum. Its TC output becomes active, locking it into the maximum state and simultaneously changing the prescaler to the lower divide ratio. The program counter continues counting up to its maximum, whereupon its TC output goes to the active state to enable the Preset mode and start a new operation cycle.

It is important to note that the divide ratio M of the program counter determines how many f_2 pulses there are in a complete program cycle; the swallow counter isn't involved. The role of the swallow counter is to modify, within limits, the number of f_1 pulses into the prescaler that are required to produce the M pulses of f_2.

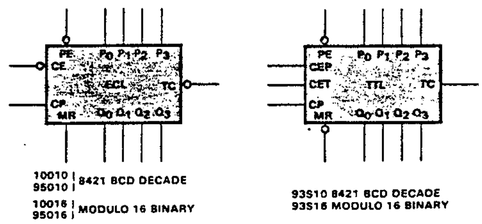


Fig. 2. Examples of Programmable Counters

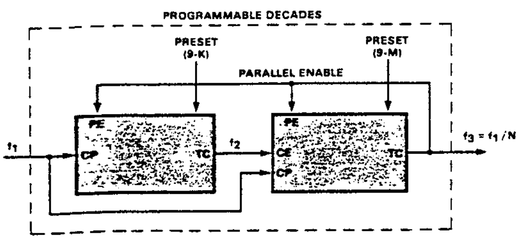


Fig. 3. Conventional Programmable Divider

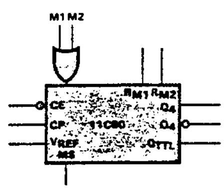
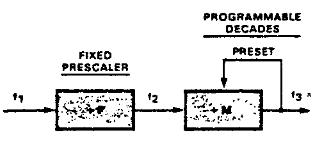


Fig. 5. Variable Modulus ÷ 10/11 650 MHz Prescaler



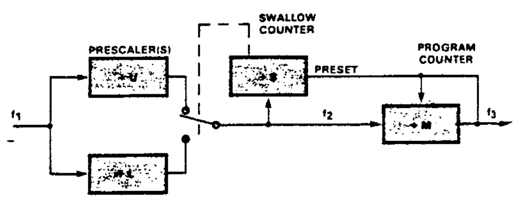


Fig. 4. Fixed Prescaler Used to Reduce Frequency

Fig. 6. Simulated Function of a Swallow Counter

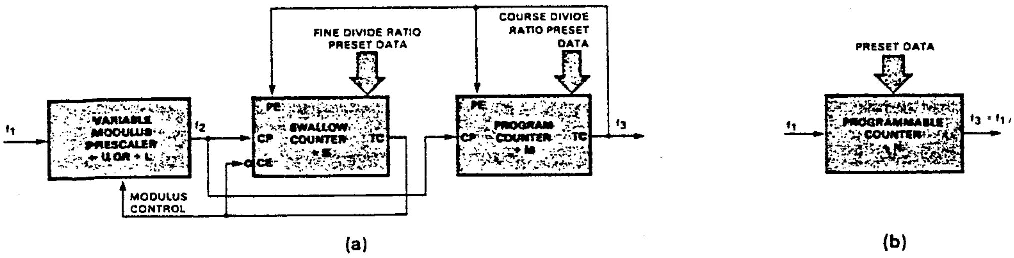


Fig. 7. Pulse Swallowing Counter and Equivalent System Building Block

The divide ratios are summarized as follows:

U = upper (larger) divide ratio of the prescaler
L = lower divide ratio of the prescaler
S = divide ratio of the swallow counter
= number of times the prescaler divides by U in a complete program cycle
M = divide ratio of the program counter
= total number of prescaler cycles in a complete program cycle

From these definitions, the number of times the prescaler divides by its lower ratio in one program cycle can be determined.

M-S = number of times the prescaler divides by L in a complete program cycle

The number of f_1 pulses that occur in each of the prescaler modes during a complete program cycle can be stated as follows:

U•S = number of f_1 pulses into the prescaler during its upper mode

L(M-S) = number of f_1 pulses into the prescaler during its lower mode

U•S + L(M-S) = total number of f_1 pulses into the prescaler during a complete program cycle

Figure 7b shows the pulse swallowing programmable counter as a single functional block, and the overall divide ratio N can be stated from the above definitions.

$$N = f_1 / f_3 = U \cdot S + L(M-S) \qquad (5)$$

Alternatively:

$$N = (U-L)S + LM \qquad (6)$$

In *Figure 7a*, the preset data inputs suggest that S and M are fine and course program controls respectively. The effect of changing S can be determined by letting S increase by one and the subtracting *Equation 6*.

$$\begin{aligned} N' &= (U-L)(S+1) + LM \\ &= (U-L)S + LM + (U-L) \\ \Delta N &= N' - N = U-L \end{aligned}$$

And in the general case:

$$\Delta N = (U-L)(\Delta S) \qquad (7)$$

Equation 7 offers some insight into why the most popular variable modulus prescalers have divide ratios such as 10/11 and 5/6. U and L differ only by one and changing S by a certain amount changes N by the same amount. Thus the combination of the prescaler and the swallow counter acts like a single, very fast, fully programmable divider. A similar analysis with M as the variable shows that the smallest adjustment afforded by the program counter is L.

$$\begin{aligned} N' &= (U-L)S + L(M+1) \\ &= (U-L)S + LM + L \\ \Delta N &= N' - N = L \end{aligned}$$

And in the general case:

$$\Delta N = L(\Delta M) \qquad (8)$$

Combining *Equations 7* and *8* gives an expression for the effects of changing either or both S and M.

$$\Delta N = (U-L)(\Delta S) + L(\Delta M) \qquad (9)$$

Notice that if U is 11 and L is 10, *Equation 9* is the same as *Equation 2* and *Equation 6* is the same as *Equation 1*, since the swallow counter of *Figure 7* and the first stage of *Figure 3* are the same type of circuit; thus S and K have the same meaning. Using 10 for L also means that the program counter can be made up of cascaded decade counters, with each decade corresponding to a decimal digit of the total divide ratio N. This is best shown by a numerical example.

To get N = 4367
with U = 11
and L = 10,
make S = 7
and M = 436

As a check, substitute these values into *Equation 5*.

$$\begin{aligned} N &= U \cdot S + L(M-S) \\ &= (11)7 + 10(436-7) = 77 + 4290 \\ &= 4367 \end{aligned}$$

Thus, the pulse swallowing counter is programmed in the same way as the divider of *Figure 3*. A practical limitation on the pulse swallowing technique is that M cannot be less than S; otherwise the program counter would reach maximum count before the swallow counter, and the latter would not have a chance to change the divide ratio of the prescaler before being preset. The prescaler would then operate the same as the fixed prescaler of *Figure 4*. Thus with decade programming, the practical minimum divide ratio for a pulse swallowing counter is 90.

CODING SYSTEM OF FAILURE REPORTING FOR QUALITY ASSESSMENT OF T & M INSTRUMENTS
(excl. potentiometric recorders)

The information contents of the coded failure description is necessary for our computerized processing of quality data.

Since the reporting of repair and maintenance routines must be complete and exact, we give you an example of a correctly filled-out PHILIPS SERVICE Job sheet.

① *Country*	② *Day Month Year*	③ *Typenumber /Version*	④ *Factory/Serial no.*
3 2	1 5 0 4 7 5	0 P M 3 2 6 0 0 2	D 0 0 0 7 8 3

CODED FAILURE DESCRIPTION ⑥

⑤ *Nature of call*

- [ ] Installation
- [ ] Pre sale repair
- [ ] Preventive maintenance
- [x] Corrective maintenance
- [ ] Other

Location	*Component/sequence no.*	*Category*
	T S 0 6 0 7	5
	R 0 0 6 3 1	2
0 0 2 1	9 9 0 0 0 1	4

⑦ *Job completed* ☒

Working time ⑧ [ ][ ][1][2] Hrs

Detailed description of the information to be entered in the various boxes:

①Country: 3 2 = Switzerland

②Day Month Year 1 5 0 4 7 5 = 15 April 1975

③Type number/Version 0 P M 3 2 6 0 0 2 = Oscilloscope PM 3260, version 02 (in later oscilloscopes this number is placed in front of the serial no)

④Factory/Serial number D 0 0 0 7 8 3 = DO 783 These data are mentioned on the type plate of the instrument

⑤Nature of call: Enter a cross in the relevant box

⑥Coded failure description

Location

[ ][ ][ ][ ]

These four boxes are used to isolate the problem area. Write the code of the part in which the fault occurs, e.g. unit no or mechanical item no of this part (refer to 'PARTS LISTS' in the manual).

Example: 0001 for Unit 1
000A for Unit A
0075 for item 75

If units are not numbered, do not fill in the four boxes; see Example Job sheet.

Component/sequence no.

[ ][ ][ ][ ][ ][ ]

These six boxes are intended to pinpoint the faulty component.

A. Enter the component designation as used in the circuit diagram. If the designation is alfa-numeric,the letters must be written (starting from the left) in the two left-hand boxes and the figures must be written (in such a way that the last digit occupies the right-most box) in the four right-hand boxes.

B. Parts not identified in the circuit diagram:

990000 Unknown/Not applicable
990001 Cabinet or rack (text plate, emblem, grip, rail, graticule, etc.)
990002 Knob (incl. dial knob, cap, etc.)
990003 Probe (only if attached to instrument)
990004 Leads and associated plugs
990005 Holder (valve,transistor, fuse, board, etc.)
990006 Complete unit (p.w. board, h.t. unit, etc.)
990007 Accessory (only those without type number)
990008 Documentation (manual, supplement, etc.)
990009 Foreign object
990099 Miscellaneous

Category

[ ]

0 Unknown, not applicable (fault not present, intermittent or disappeared)
1 Software error
2 Readjustment
3 Electrical repair (wiring, solder joint, etc.)
4 Mechanical repair (polishing, filing, remachining, etc.)
5 Replacement (of transistor, resistor, etc.)
6 Cleaning and/or lubrication
7 Operator error
8 Missing items (on pre-sale test)
9 Environmental requirements are not met

⑦Job completed: Enter a cross when the job has been completed.

⑧Working time: Enter the total number of working hours spent in connection with the job (excluding travelling, waiting time, etc.), using the last box for tenths of hours.

[ ][ ][1][2] = 1,2 working hours (1 h 12 min.)

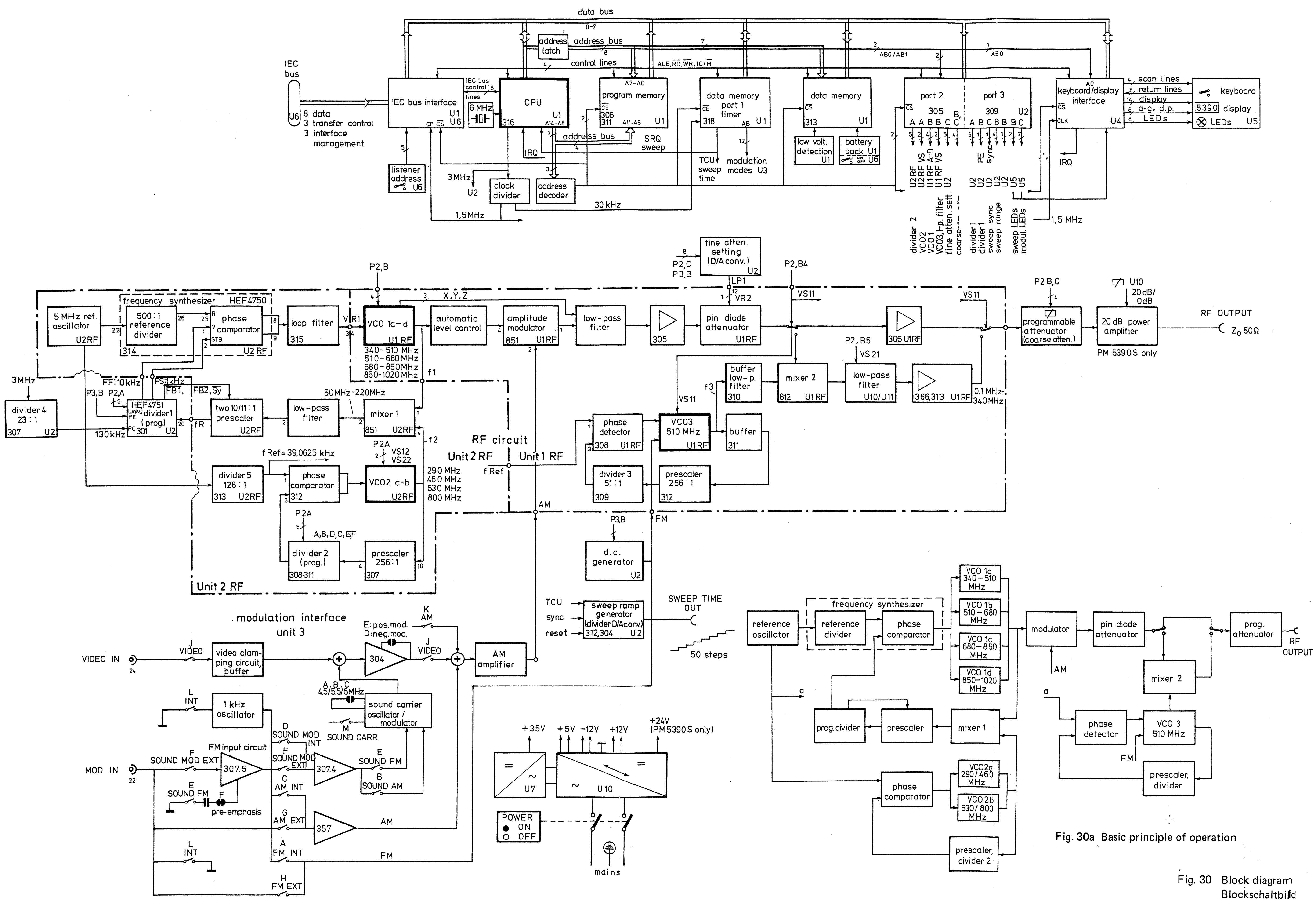


Fig. 30a Basic principle of operation

Fig. 30 Block diagram
Blockschaltbild
Schéma synoptique

Fig. 31 Front view

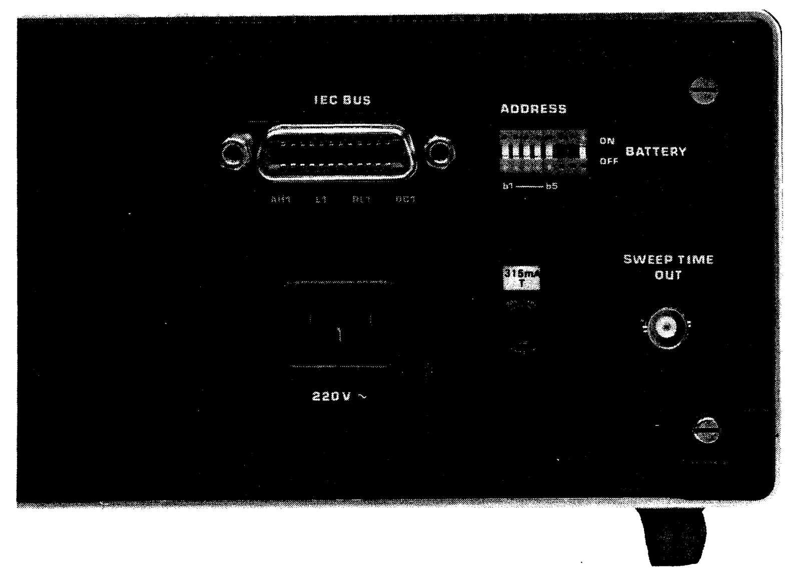


Fig. 32 Rear view

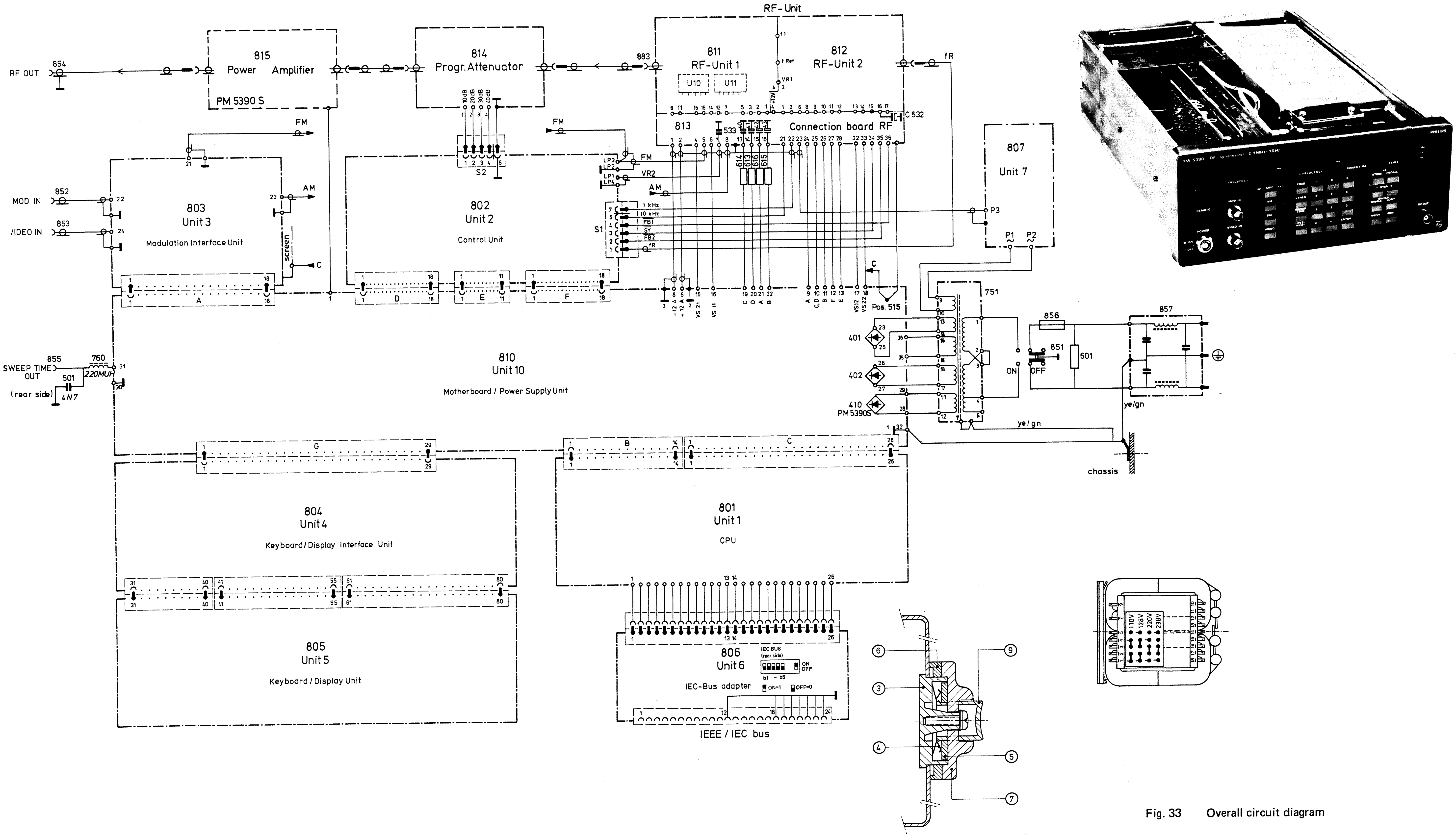
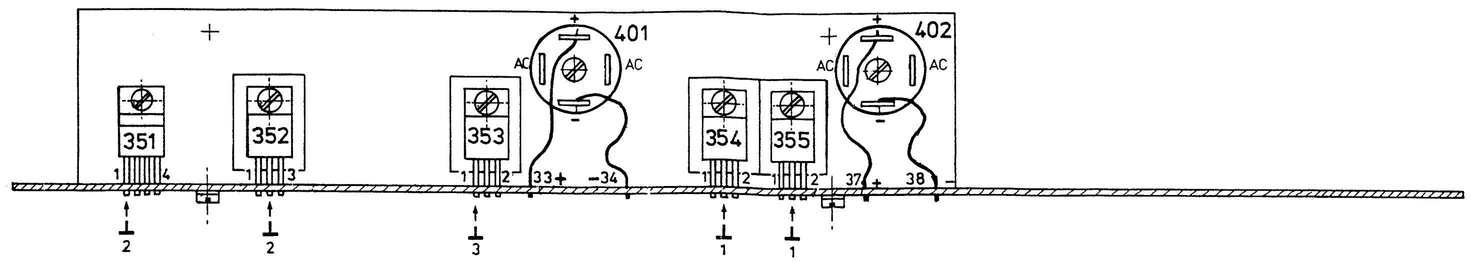
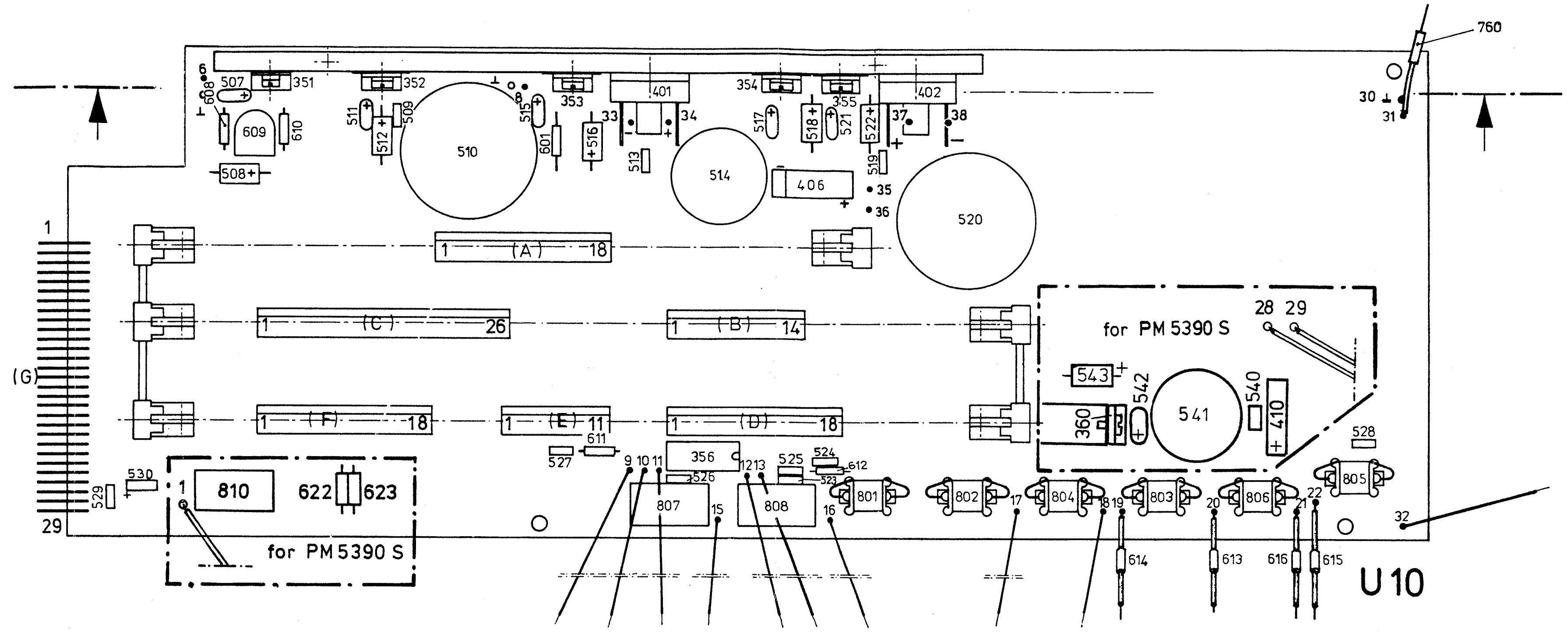
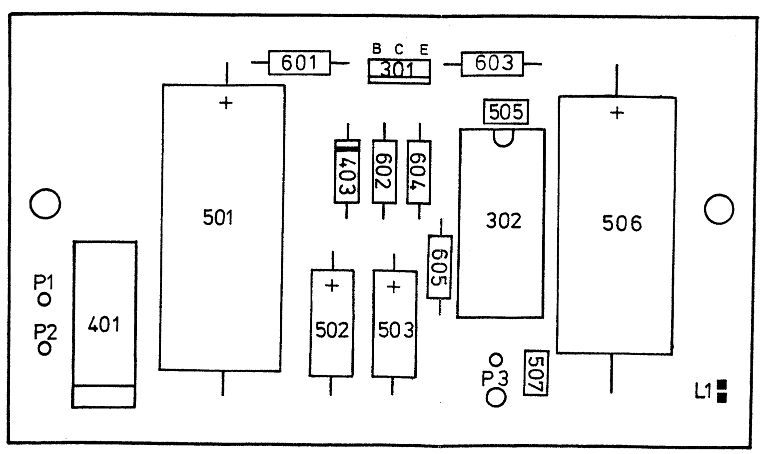


Fig. 33 Overall circuit diagram





U 10



U7

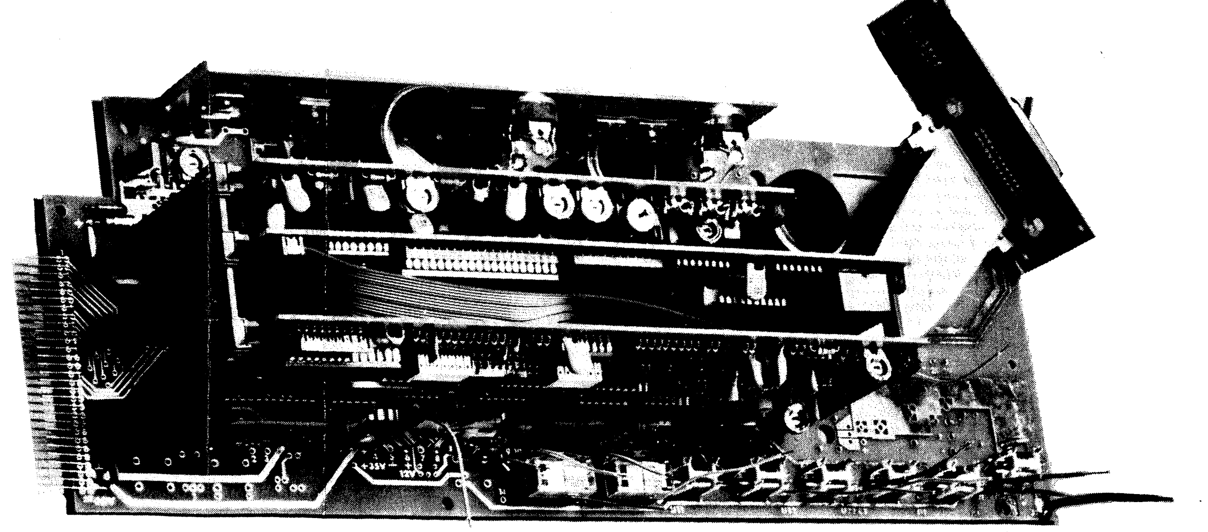


Fig. 34 Unit 10, Unit 7; Motherboard, Power supply

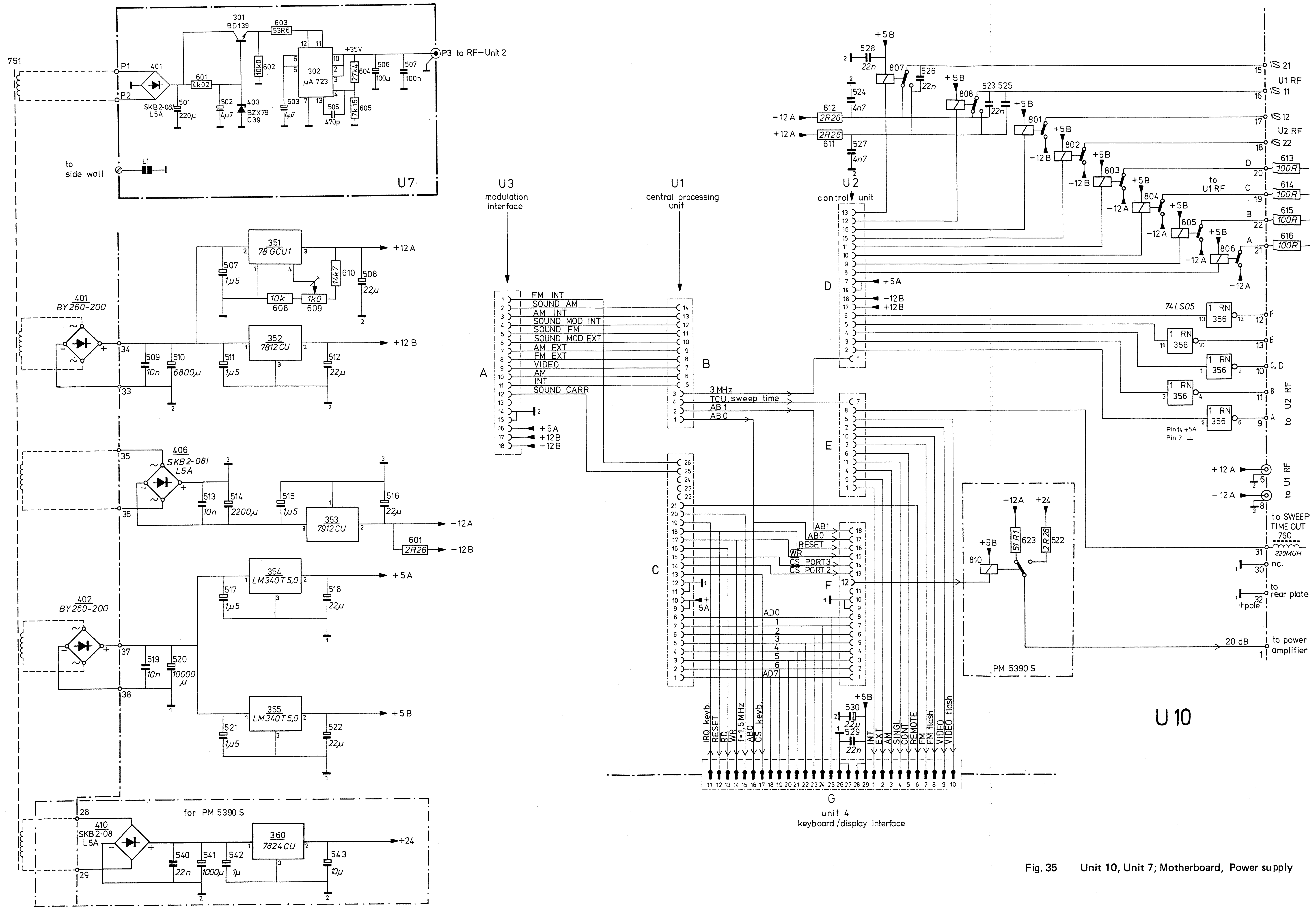
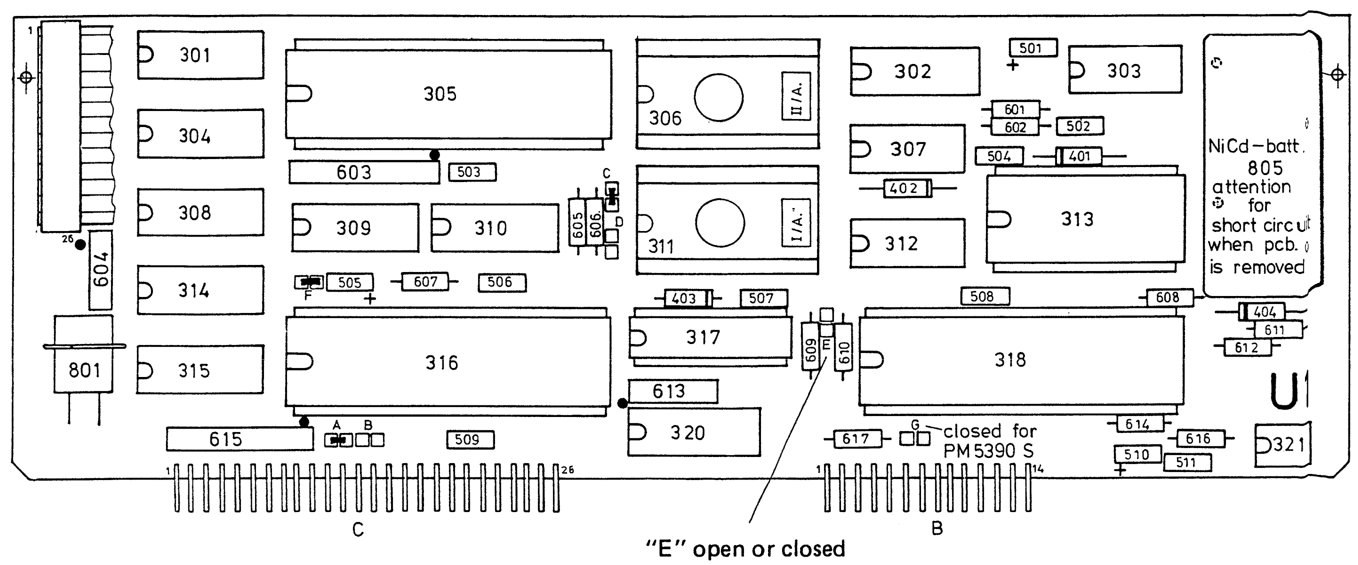


Fig. 35 Unit 10, Unit 7; Motherboard, Power supply



"E" open or closed
dependend on adjustment
(see table 7.3.1 seq. 5.2.)

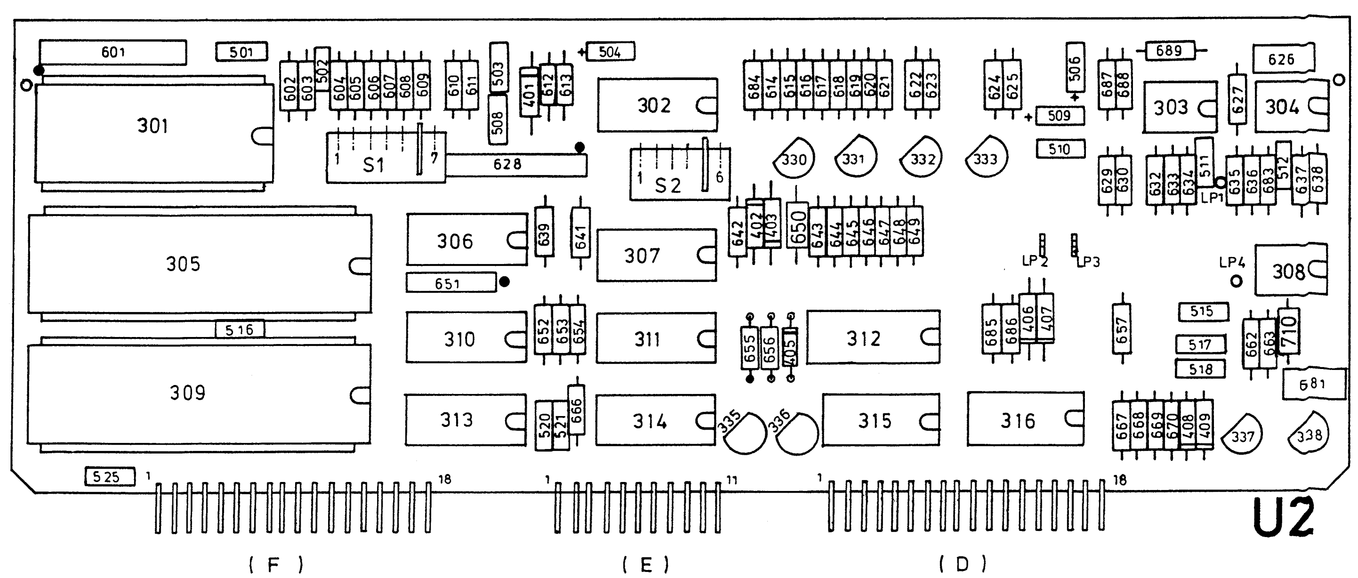
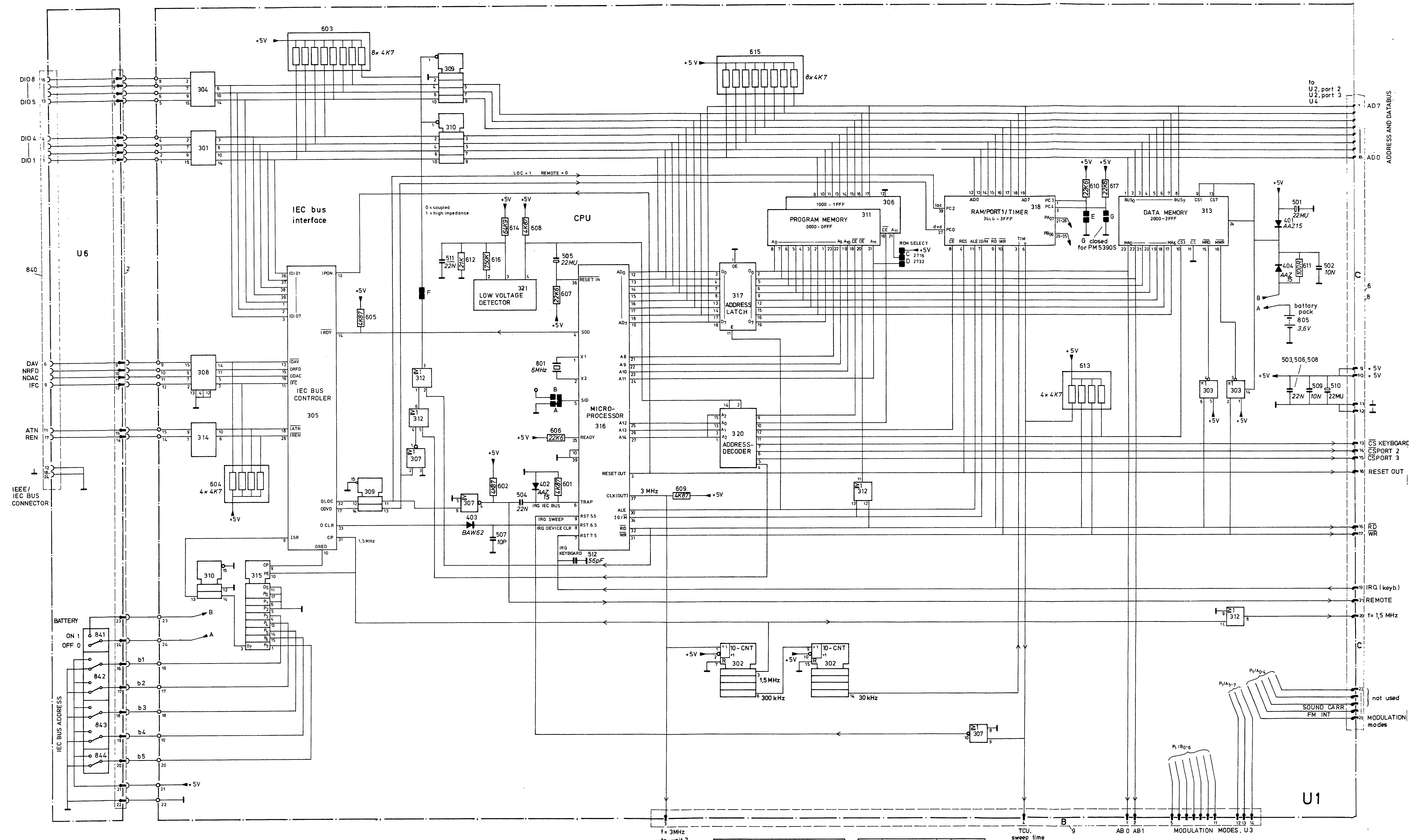


Fig. 36 Units U1 and U2: component lay -out



POS No	TYPE	PIN No Vcc5V	PIN No GND
301	MC 3441	16	8
304	MC 3441	16	8
308	MC 3441	16	8
314	MC 3441	16	8
302	HEF 4518 BP	16	8
303	HEF 4077	*	7
305	HEF 4738	40	20
309	HEF 40097 BP	16	8
310	HEF 40097 BP	16	8
311	B 2732	24	12

POS No	TYPE	PIN No Vcc5V	PIN No GND
312	74LS32	14	7
313	CDP1823E	*	12
315	HEF4014 BP	16	8
316	P8085AH	40	20
317	74LS 363	20	10
318	P8155H	40	20
306	B 2716	24	12
320	74 LS 155	16	8
321	ICL 8212 CPA	8	5
307	74LS 02	14	7

* see above

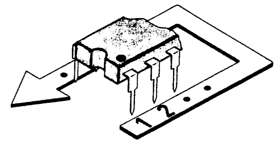
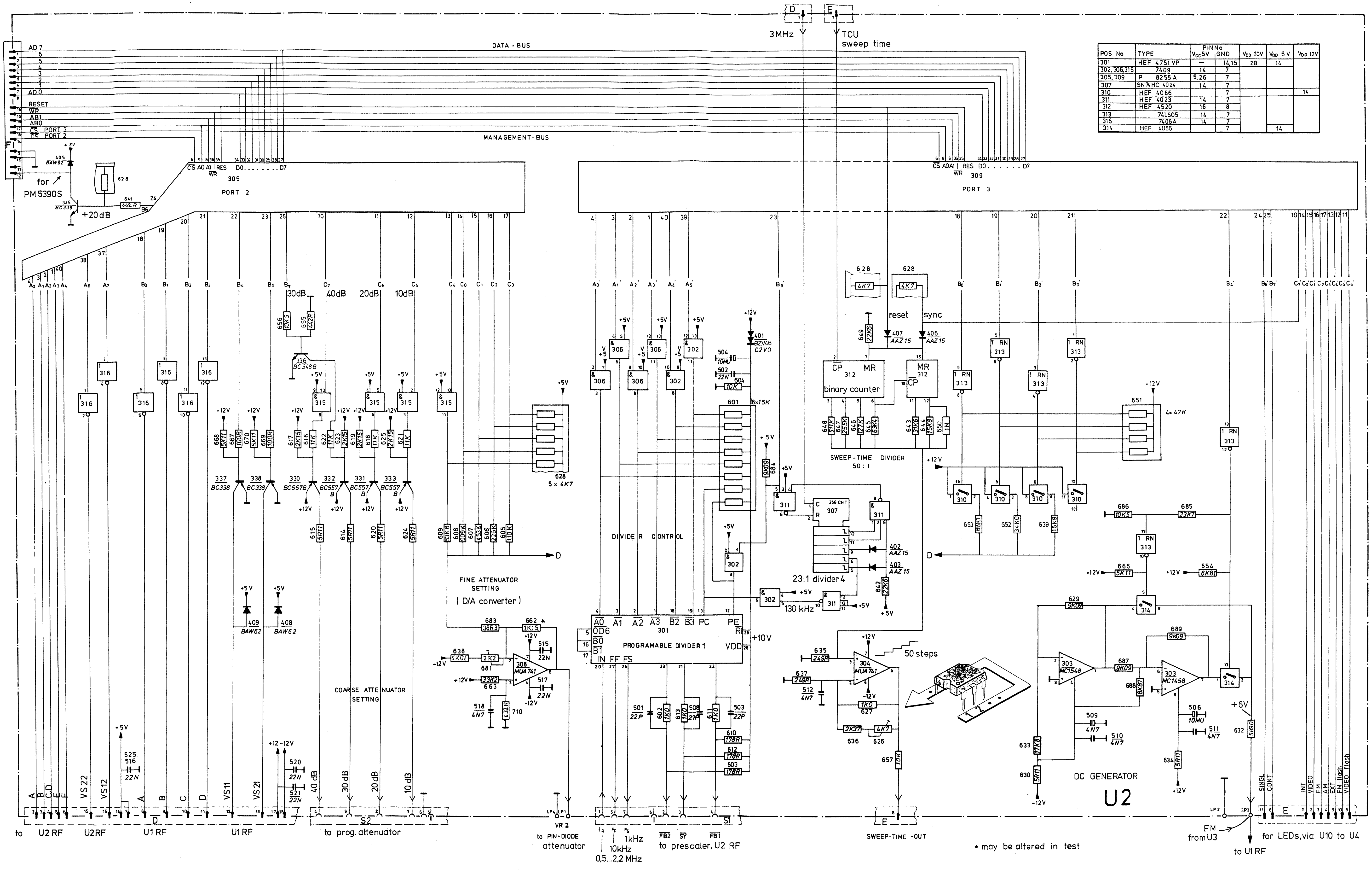
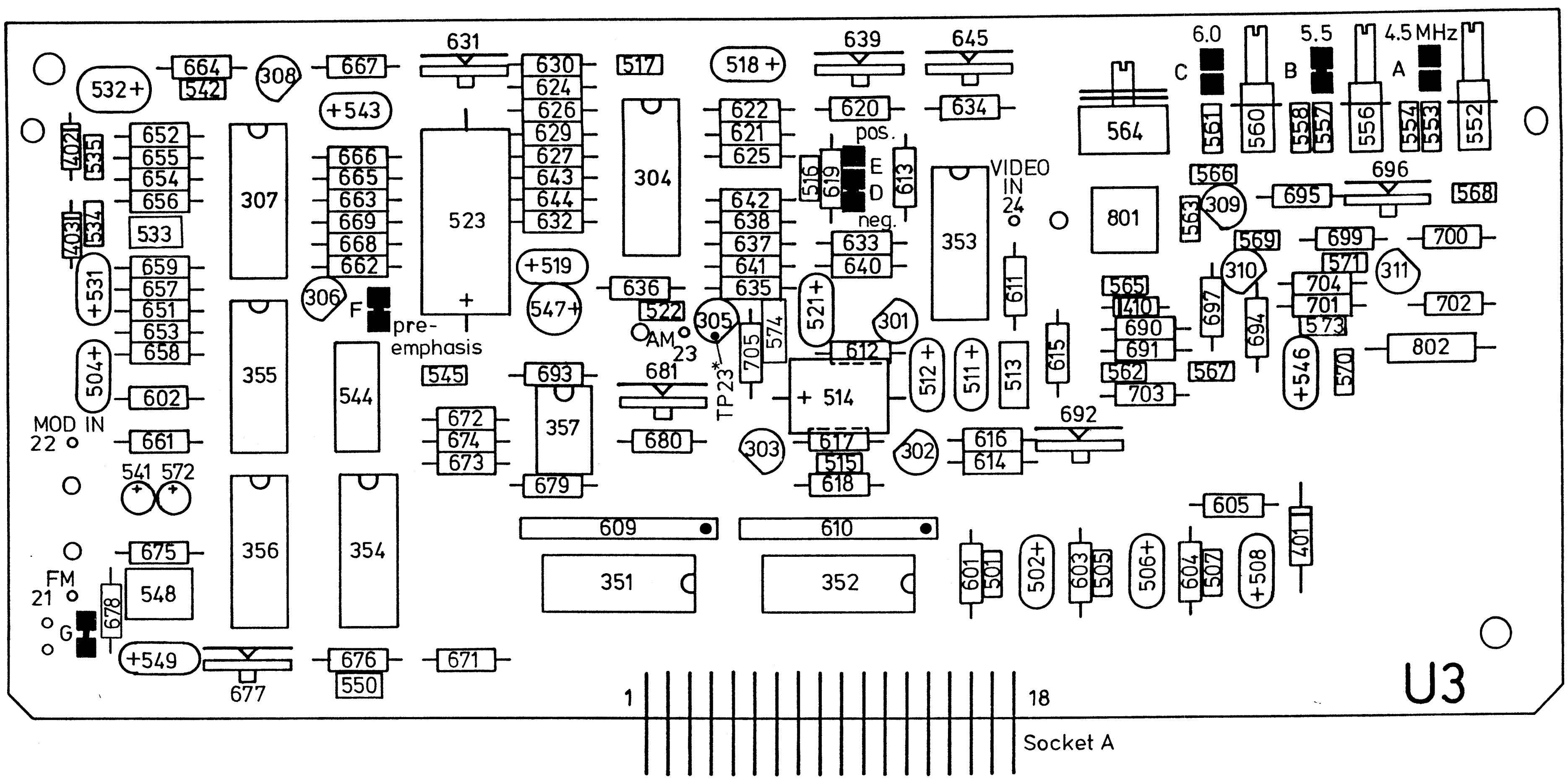


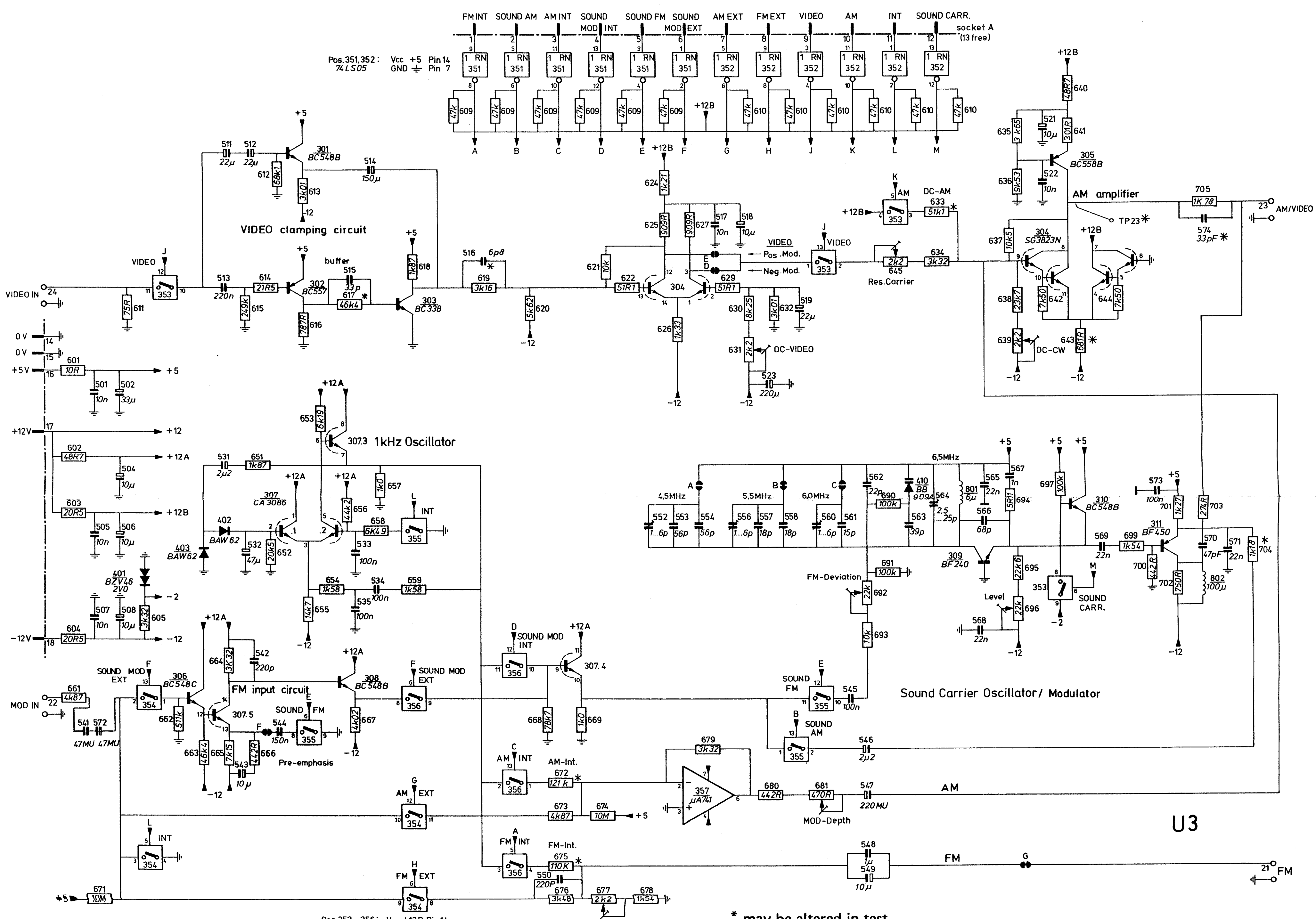
Fig. 37 Unit 1; CPU, IEC bus interface



POS No	TYPE	PIN No V_{CC} 5V	GND	V_{DD} 10V	V_{DD} 5V	V_{DD} 12V
301	HEF 4751 VP	—	14,15	28	14	
302, 306, 315	7409	14	7			
305, 309	P 8255 A	5,26	7			
307	SN74HC 4024	14	7			
310	HEF 4066		7			14
311	HEF 4023	14	7			
312	HEF 4520	16	8			
313	74LS05	14	7			
316	7406A	14	7			
314	HEF 4066		7		14	

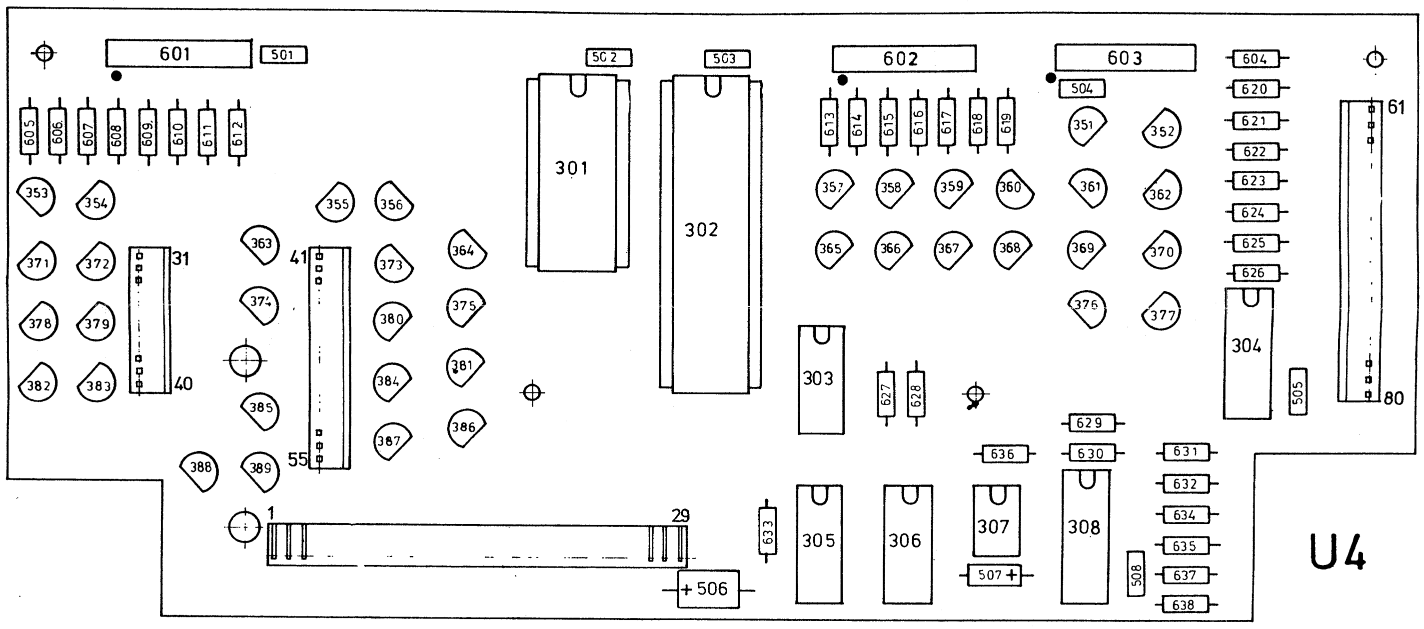
Fig. 38 Unit 2; Control unit

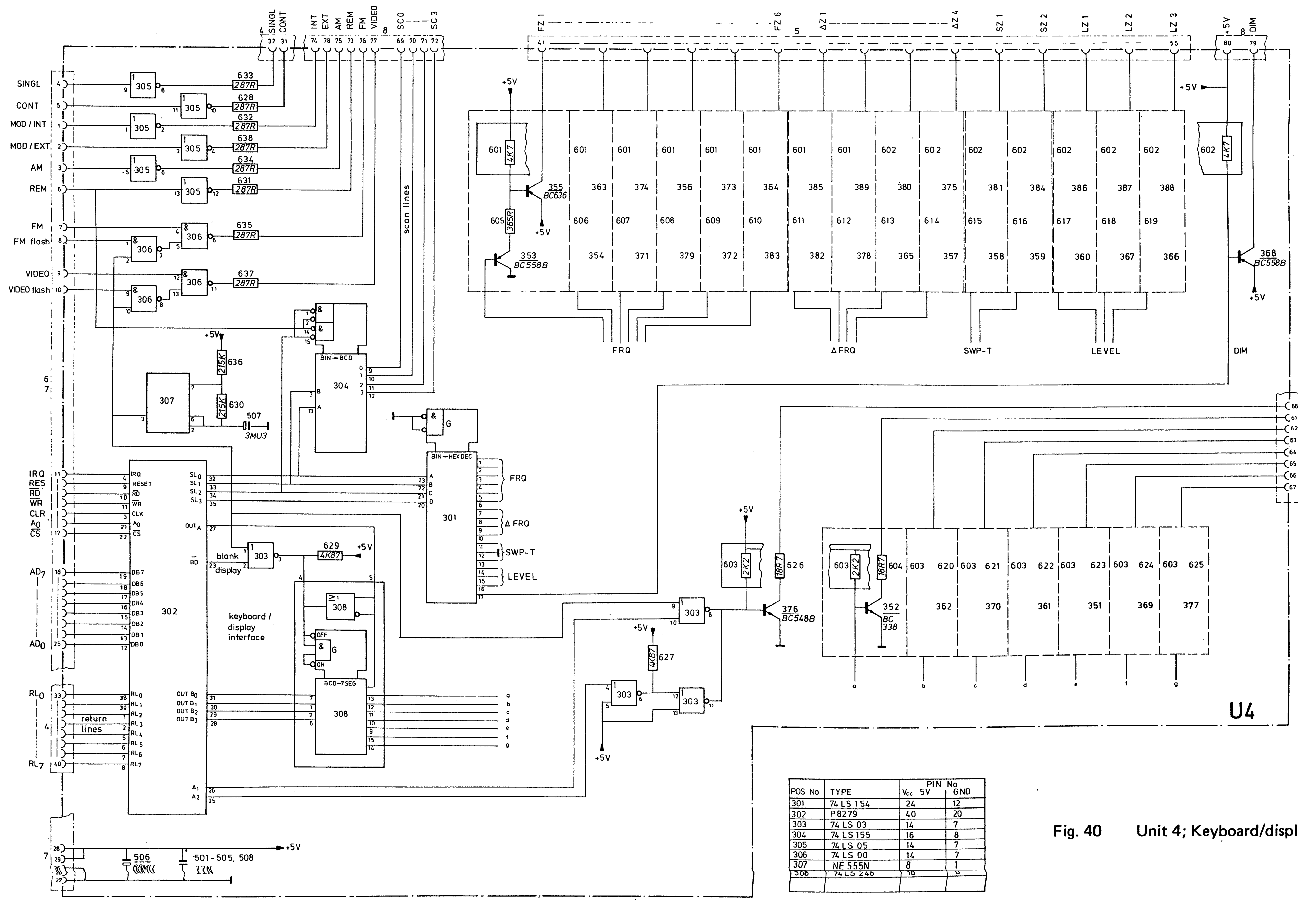




* may be altered in test

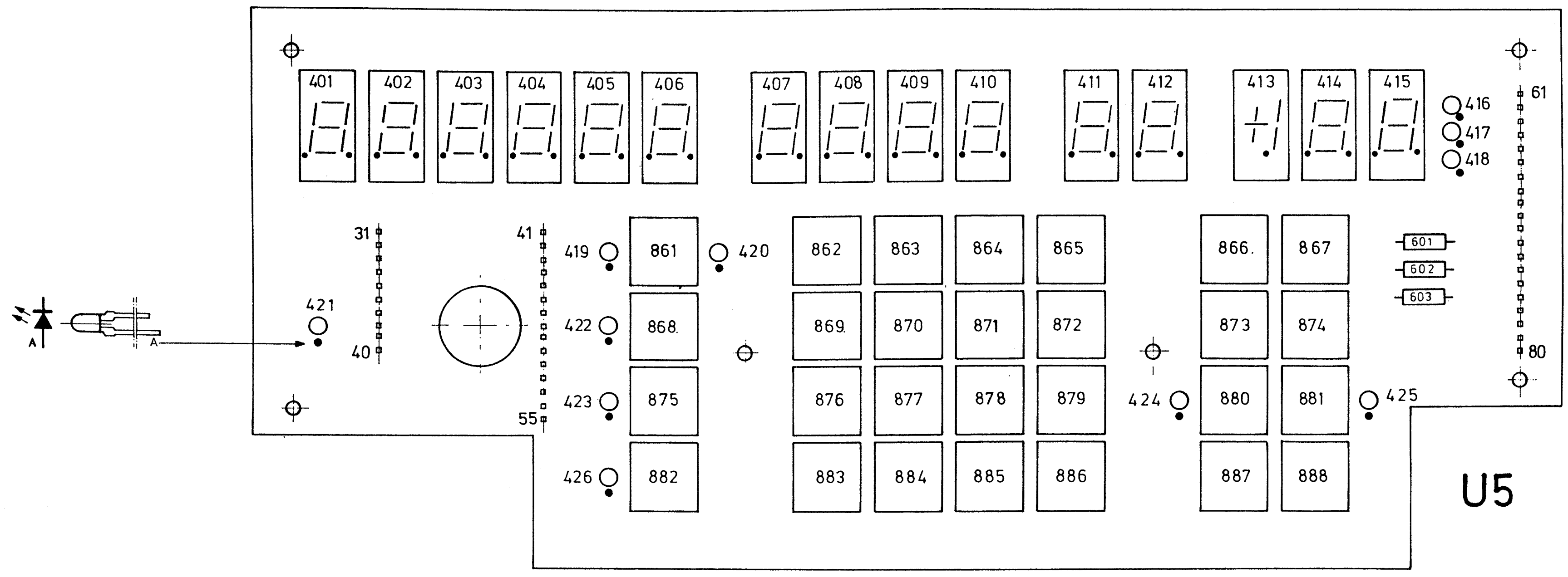
Fig. 39 Unit 3; Modulation interface





POS No	TYPE	PIN No V_{cc} 5V	GND
301	74 LS 154	24	12
302	P8279	40	20
303	74 LS 03	14	7
304	74 LS 155	16	8
305	74 LS 05	14	7
306	74 LS 00	14	7
307	NE 555N	8	1
308	74 LS 248	16	8

Fig. 40 Unit 4; Keyboard/display interface



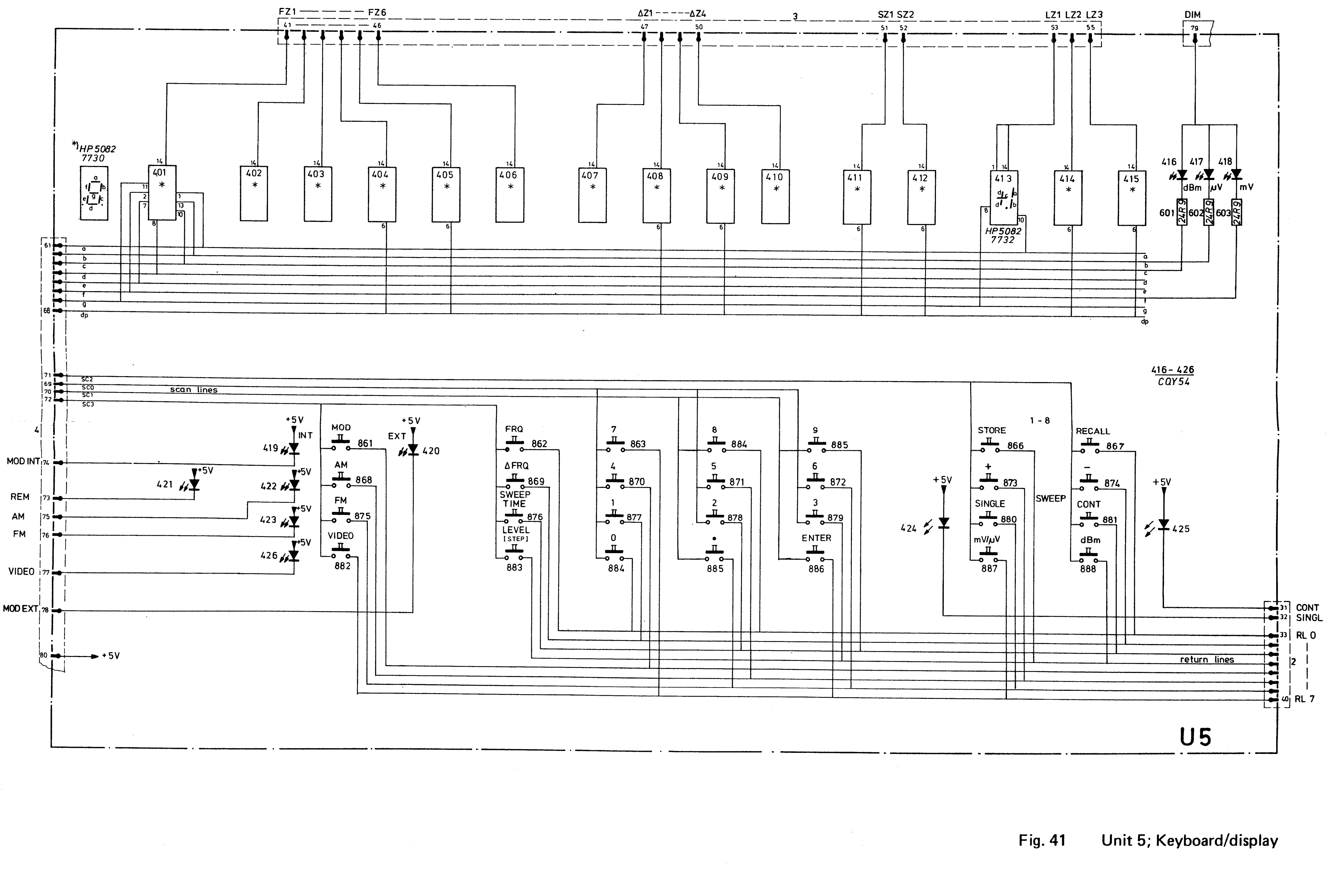
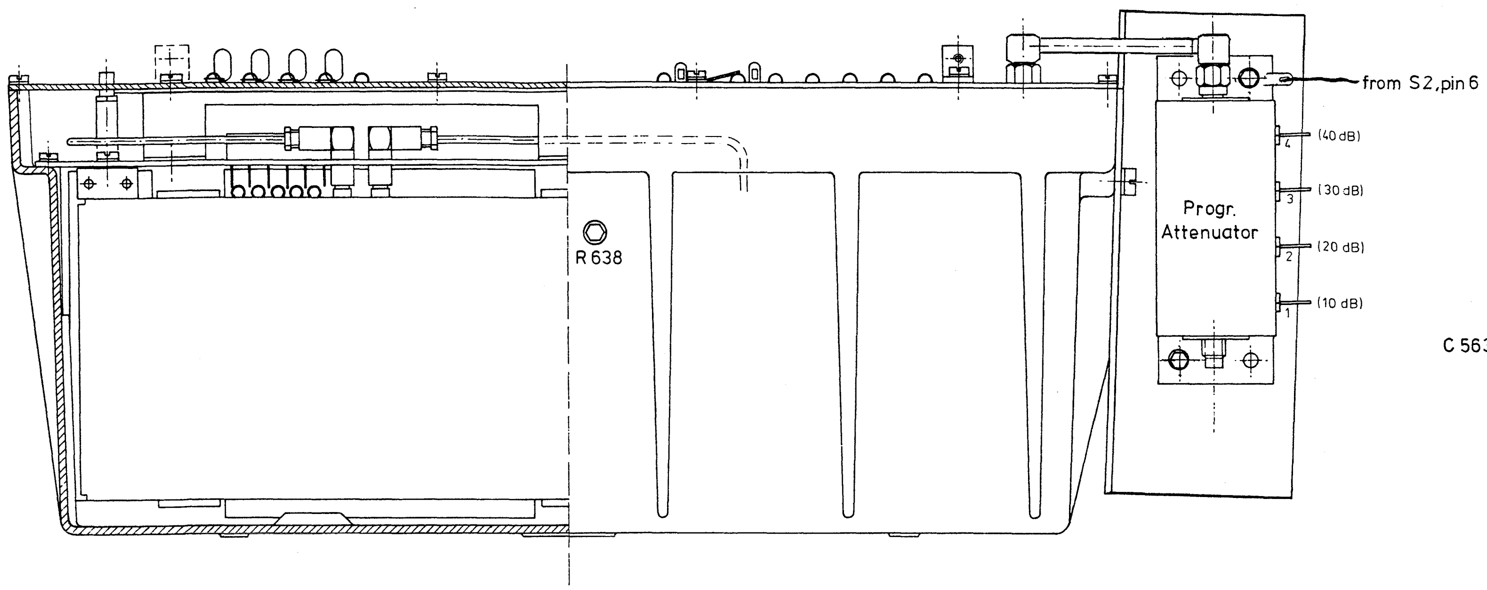
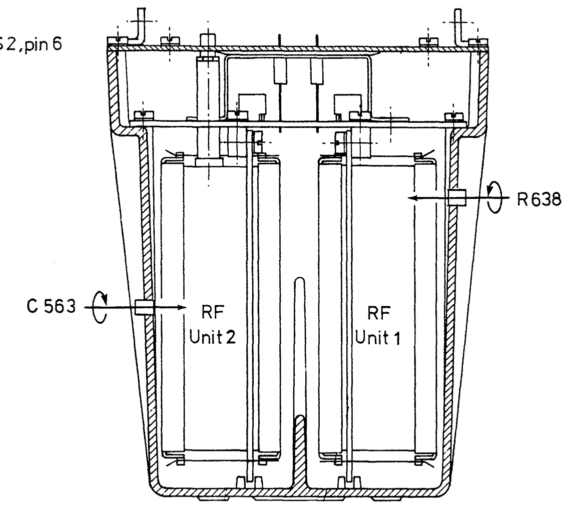
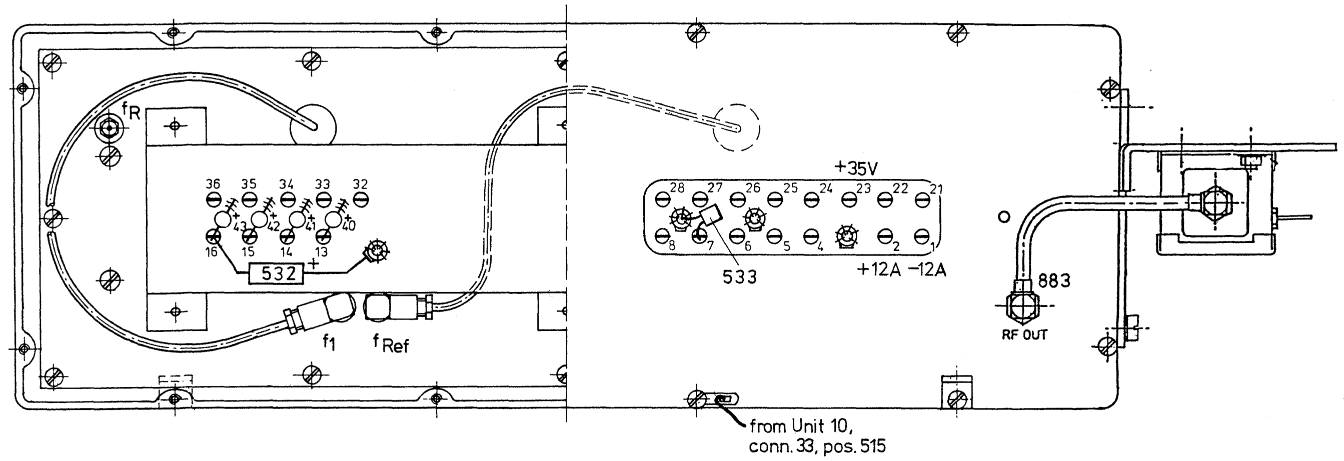


Fig. 41 Unit 5; Keyboard/display



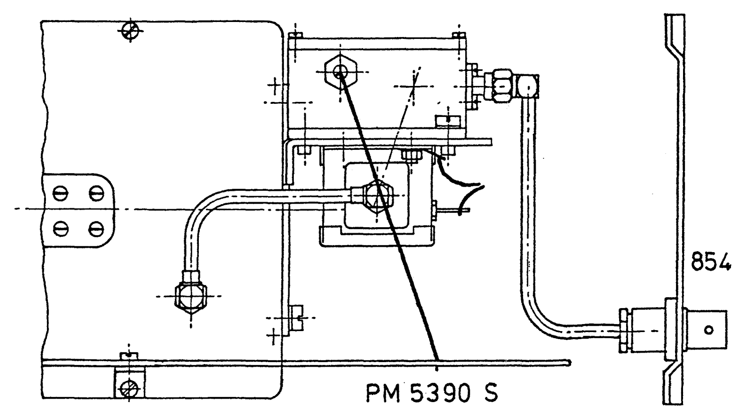




solder connections

connection RF board

	colour / comp.	RF Unit 1			colour	RF Unit 2	
1	blue	8	-12 A	21	violet	1	10 kHz
2	red	11	+12 A	22	brown	2	1 kHz
3	—			23	orange	6	+ 35 V
4	green	16	VS 21	24	white	8	div. A
5	coax	15	FM	25	grey	9	div. C, D
6	yellow	14	VS 11	26	black	10	div. B
7	coax	12	VR 2	27	brown	11	div. F
8	coax	7	AM	28	violet	12	div. E
9	—			29	—		
10	—			30	—		
11	—			31	—		
12	—			32	green	14	VS 22
13	R 614	5	VCO 1C	33	yellow	13	VS 12
14	R 613	3	VCO 1D	34	green	15	$\overline{SY}$
15	R 616	2	VCO 1A	35	yellow	16	$\overline{FB\ 2}$
16	R 615	1	VCO 1B	36	orange	17	$\overline{FB\ 1}$
/	—	4	VR 1	/	—	3	VR 1
						4	+12 V



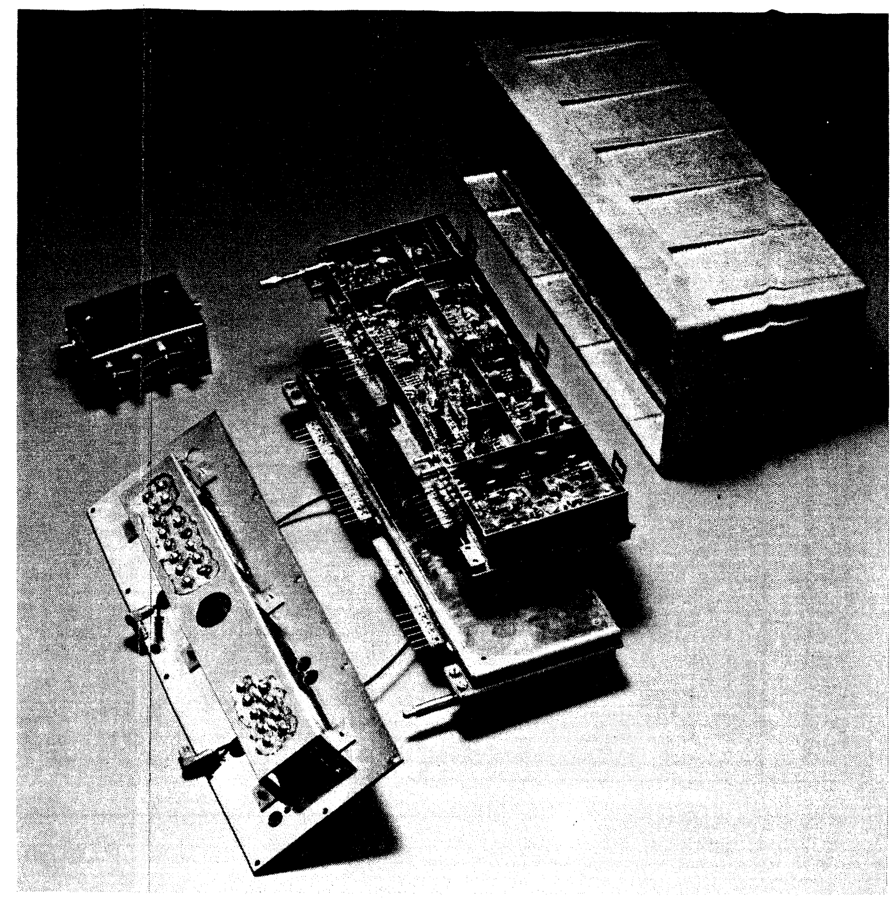
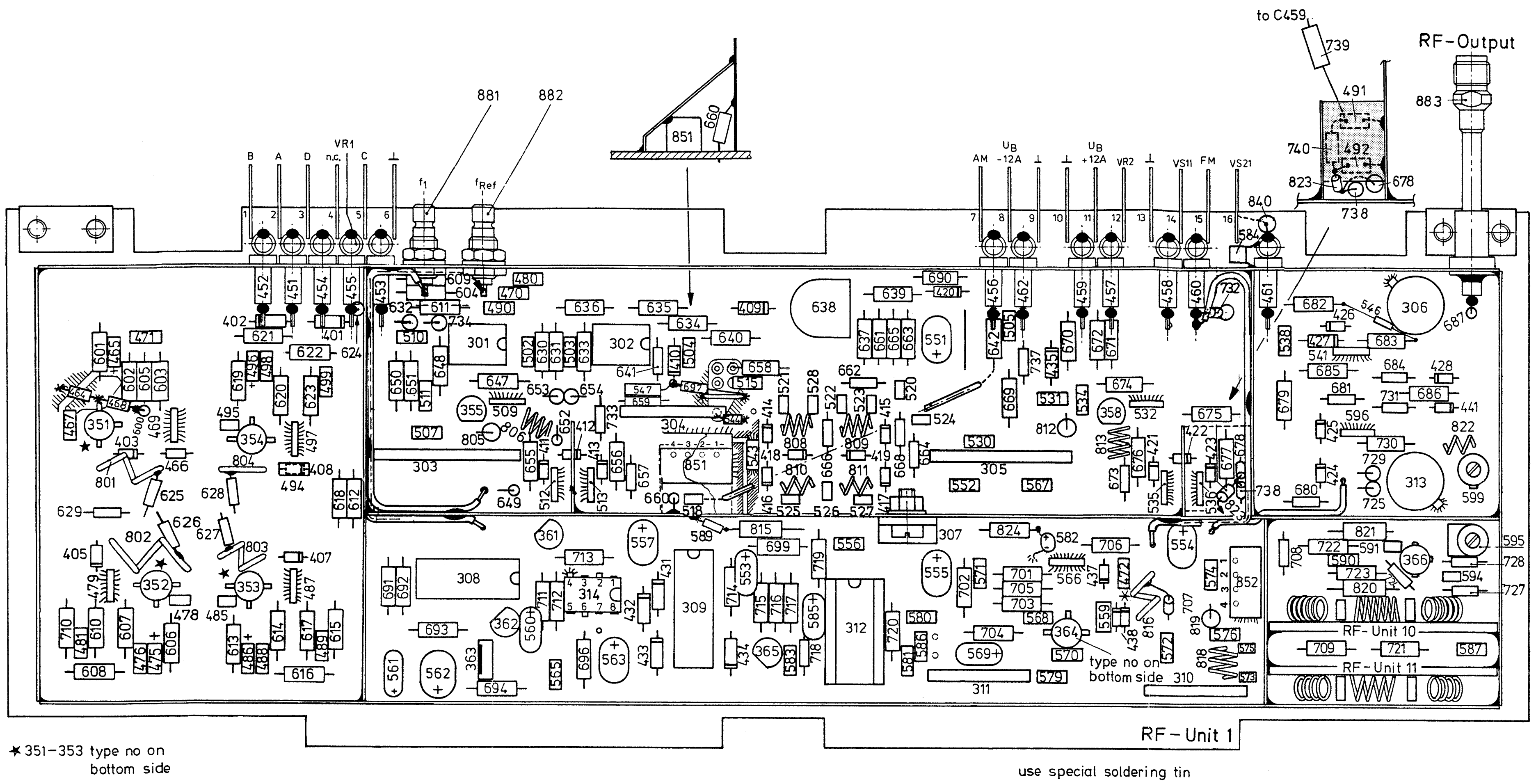
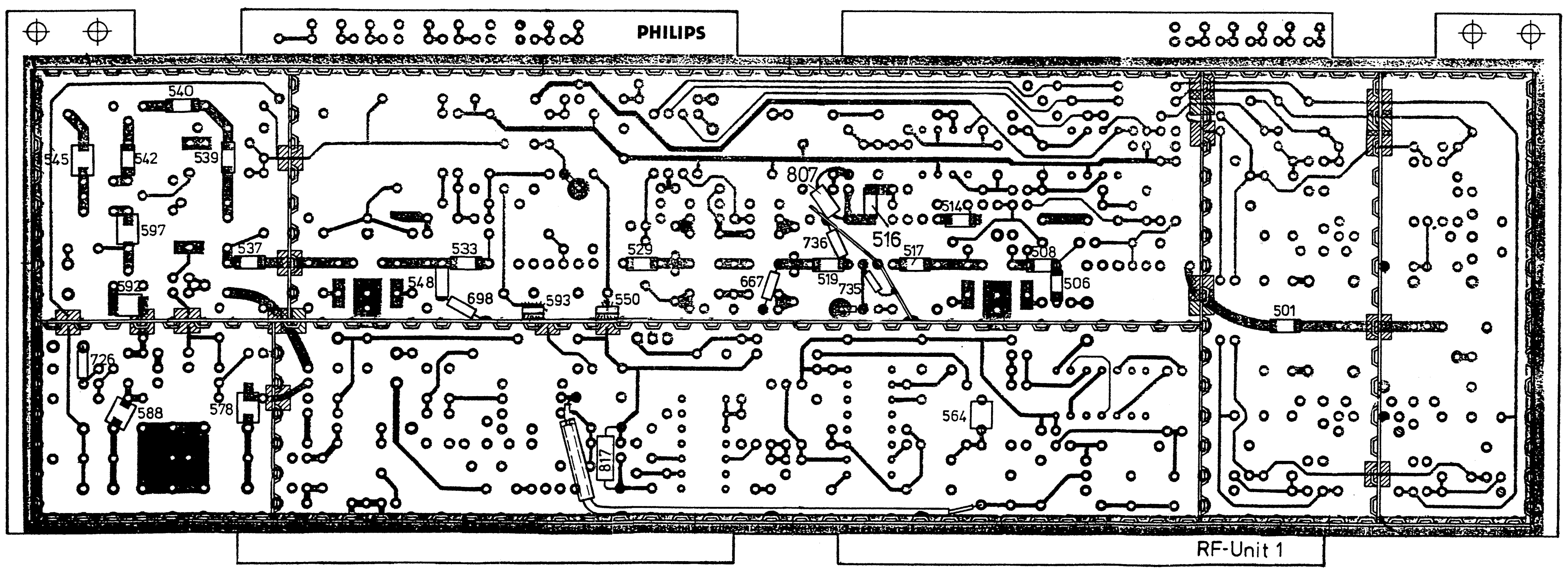
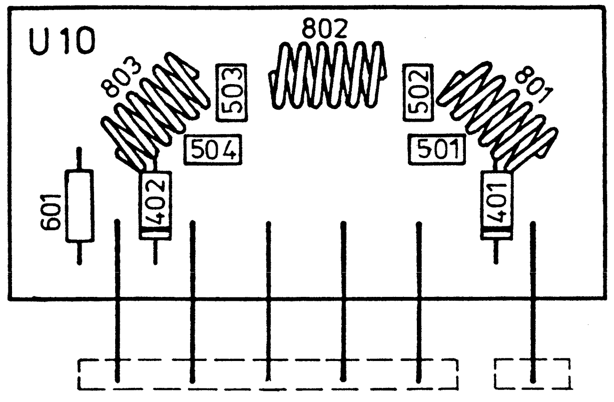


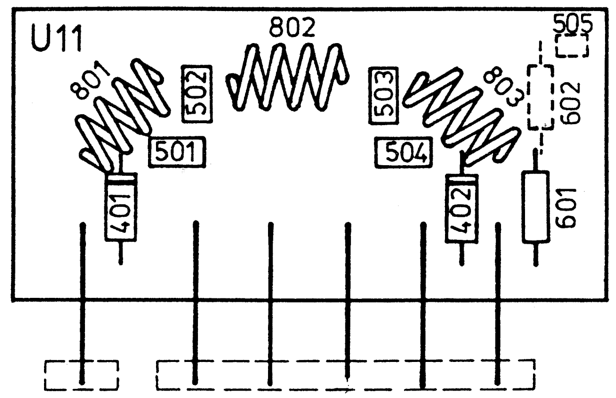
Fig. 42 RF units mounted





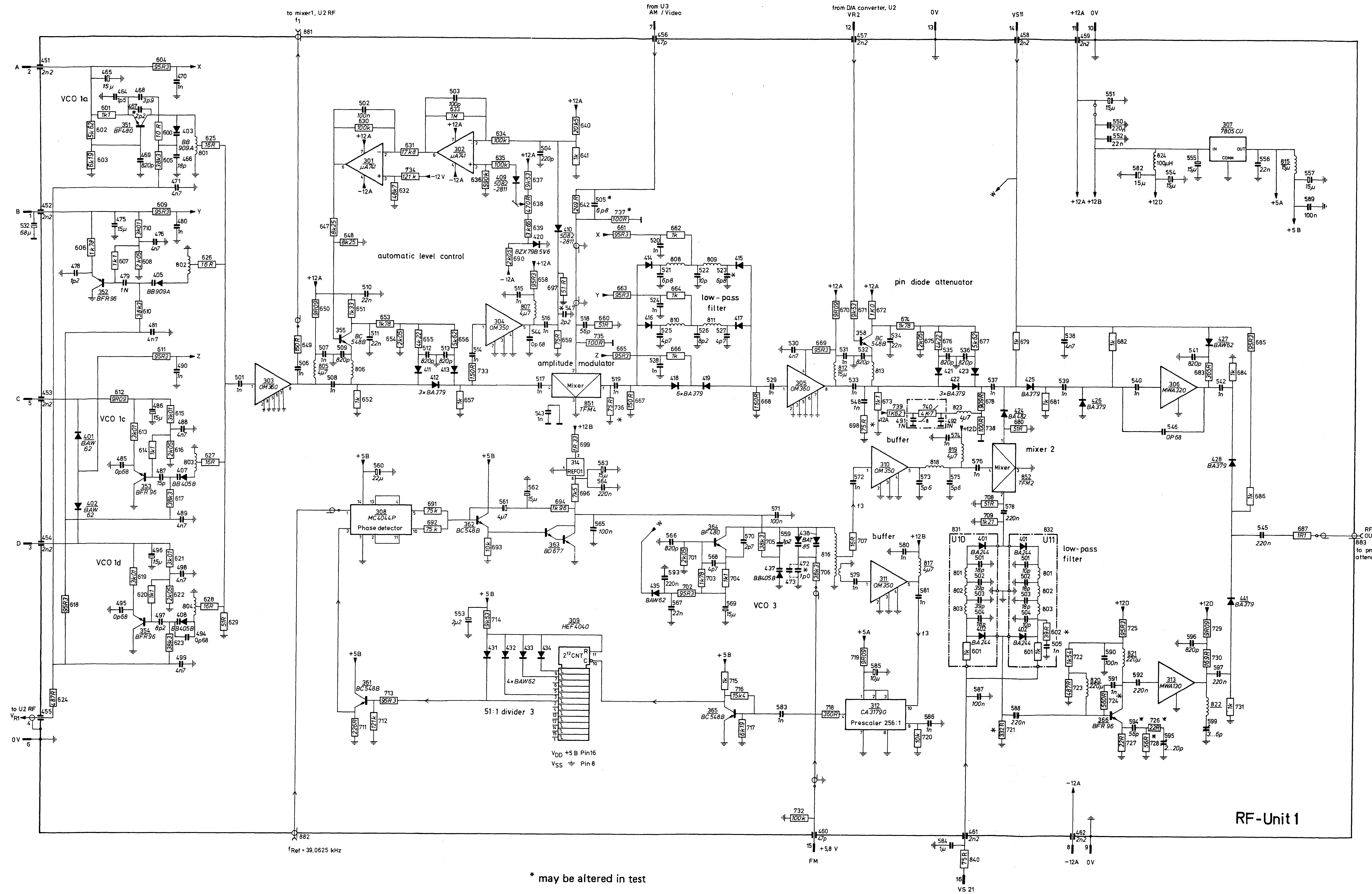


Unit 10 on RF-U1



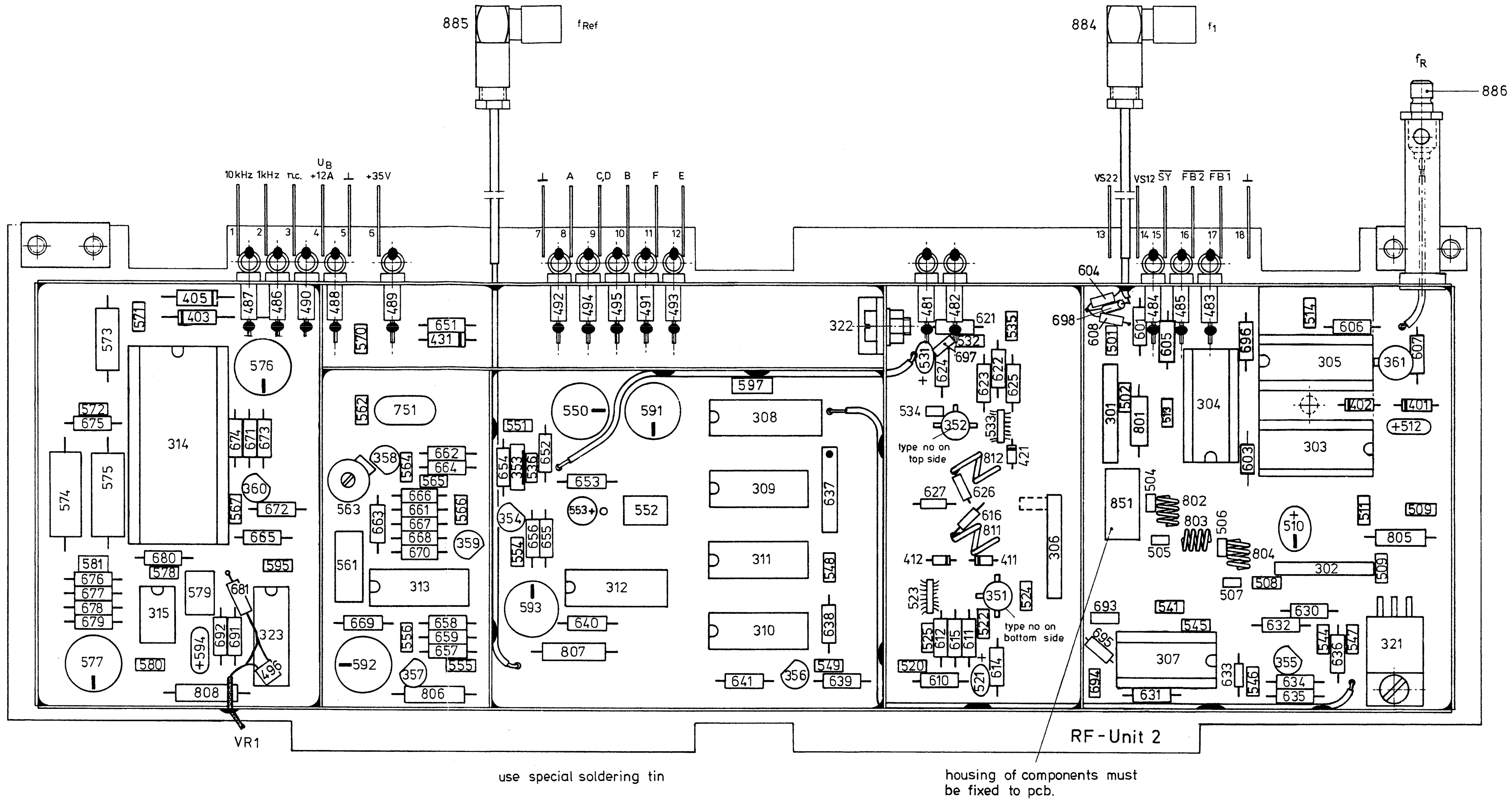
Unit 11 on RF-U1

Fig. 43 RF unit 1: component lay-out



* may be altered in test

Fig. 44 RF unit 1



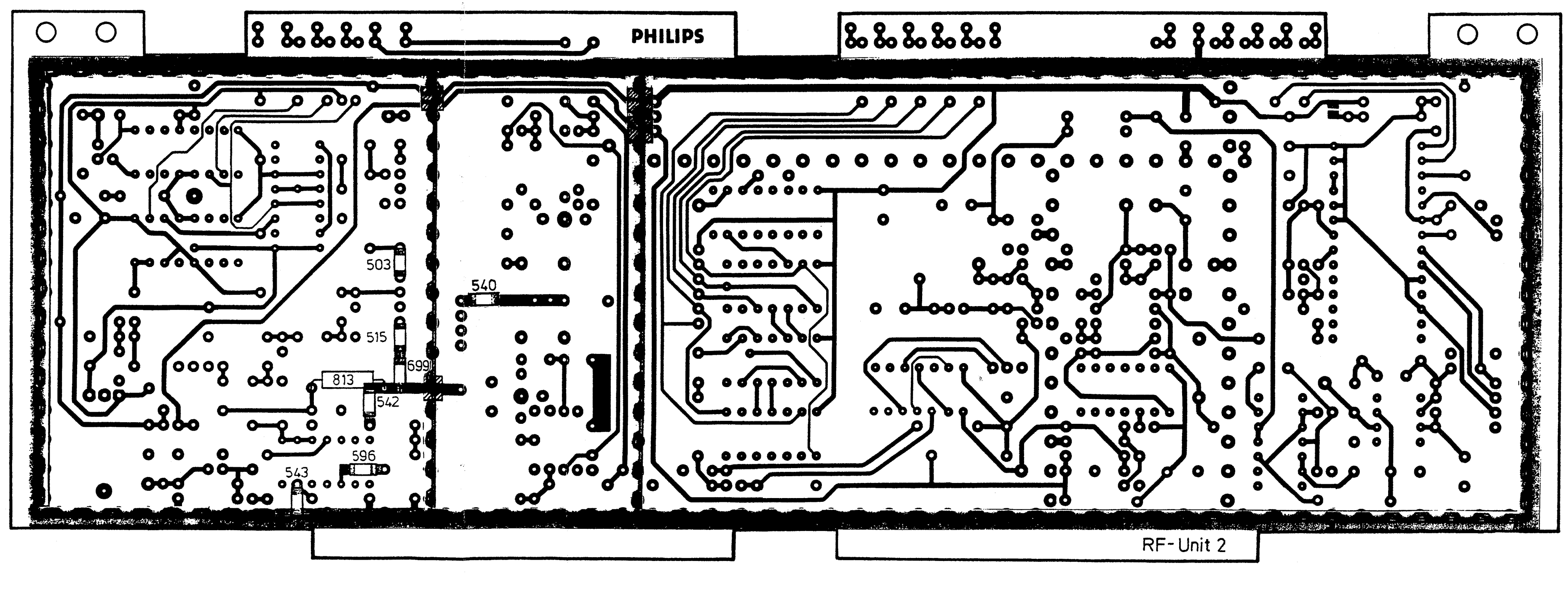
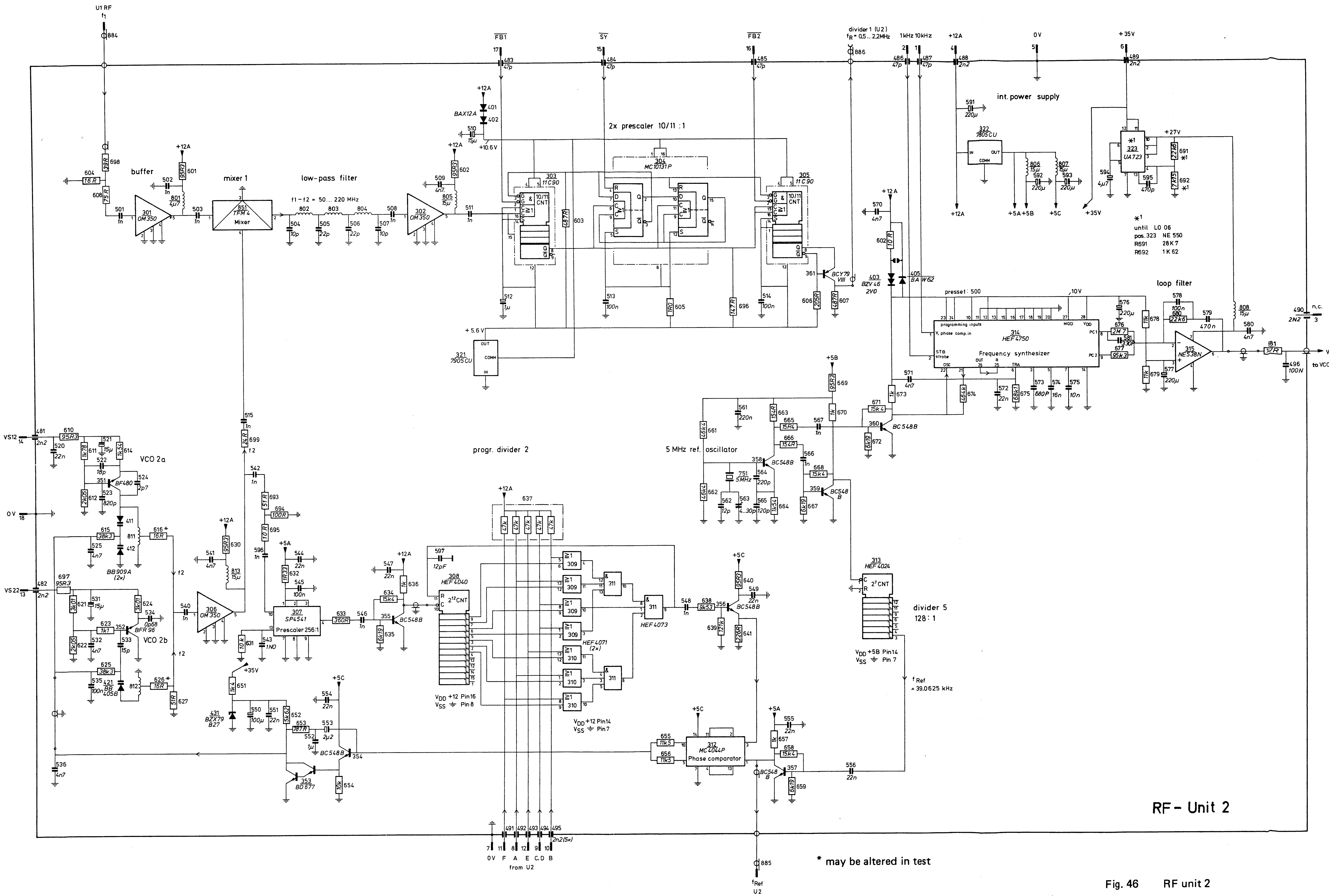
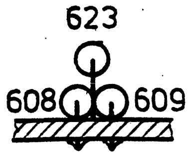


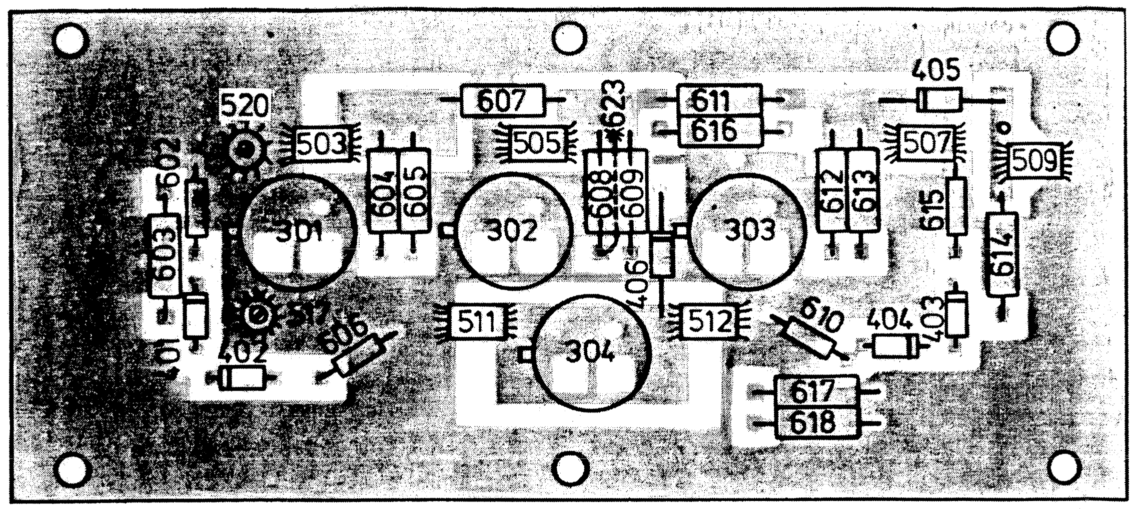
Fig. 45 RF unit 2: component lay-out



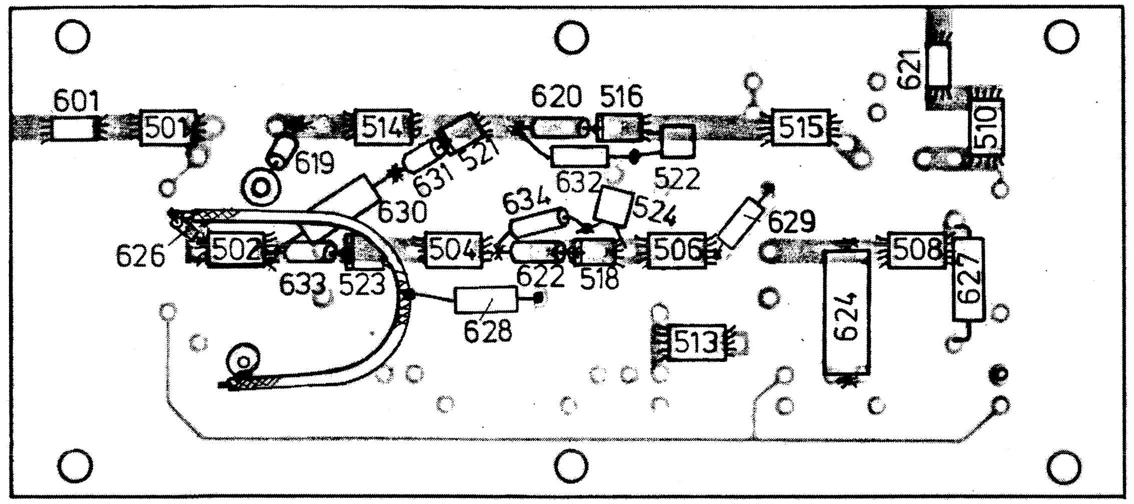
* may be altered in test

Fig. 46 RF unit 2

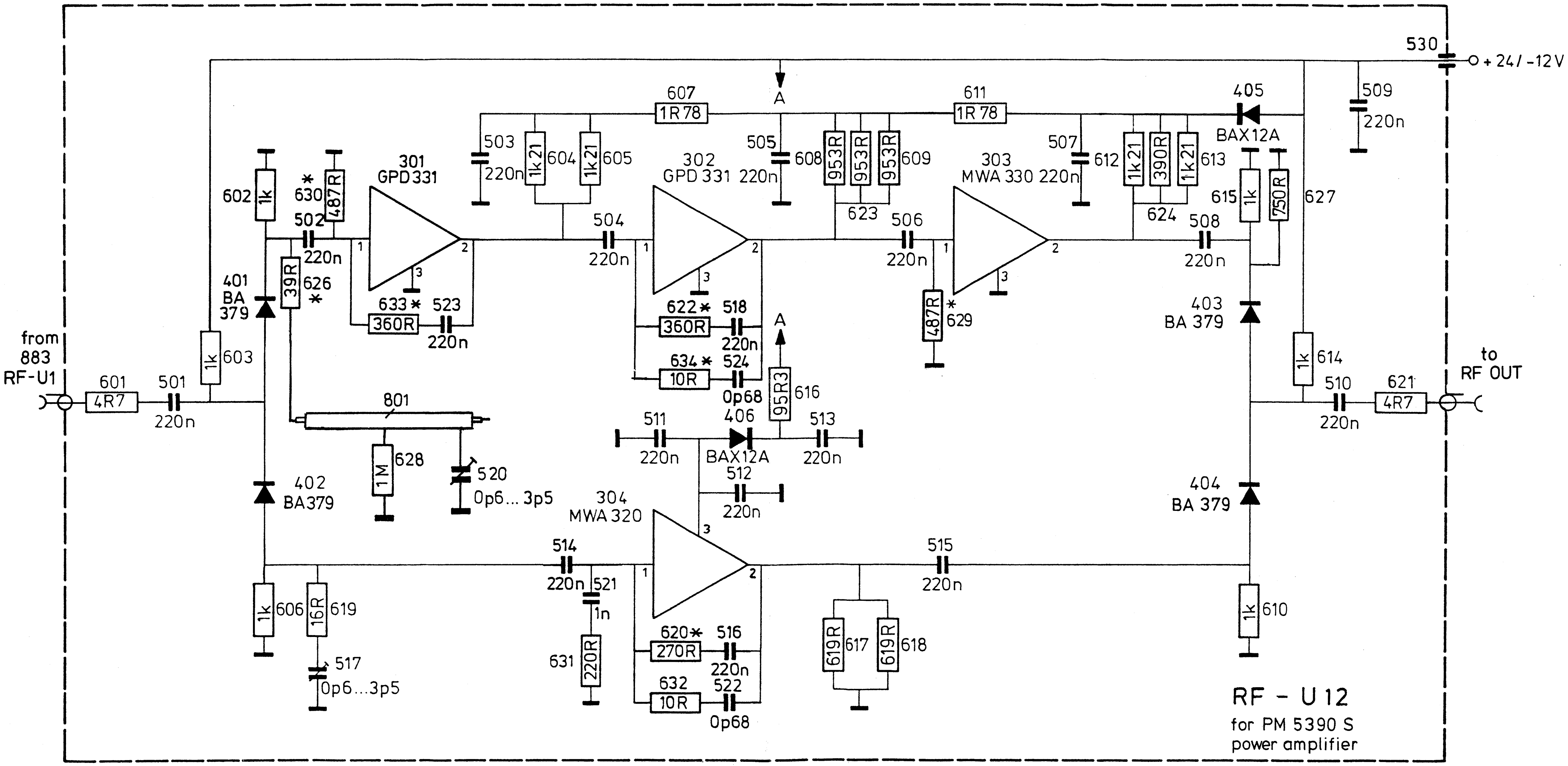




Pos. 301 . . . 304 must be fixed to pcb



Pos. 619, 620, 622: wires as short as possible



* may be altered in test

Fig. 47 RF unit 12: power amplifier

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